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MAY 10

Issue 10/2007

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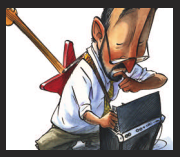

INTERFACE OVERKILL?

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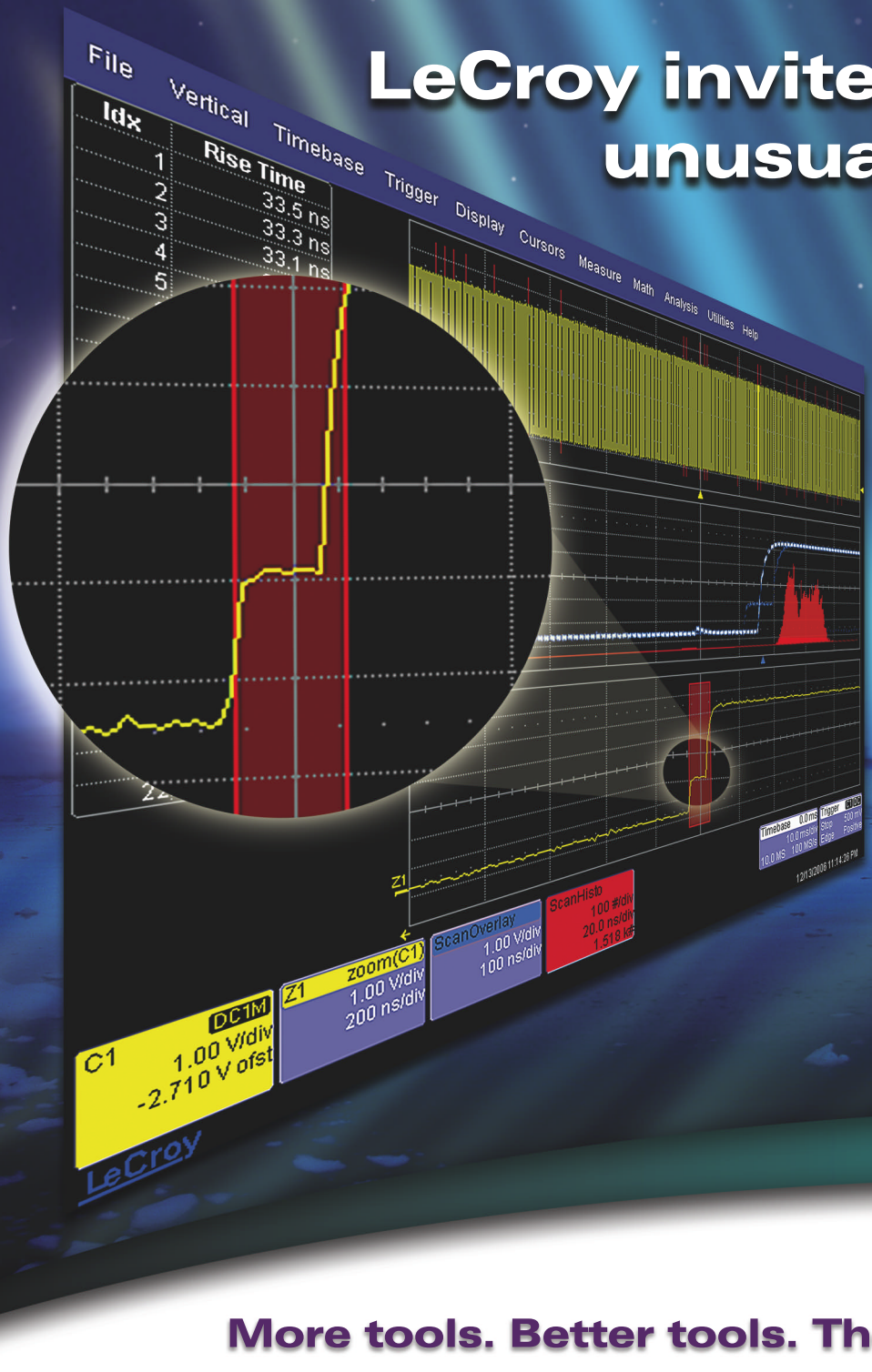
LeCroy invites you to unusual events.



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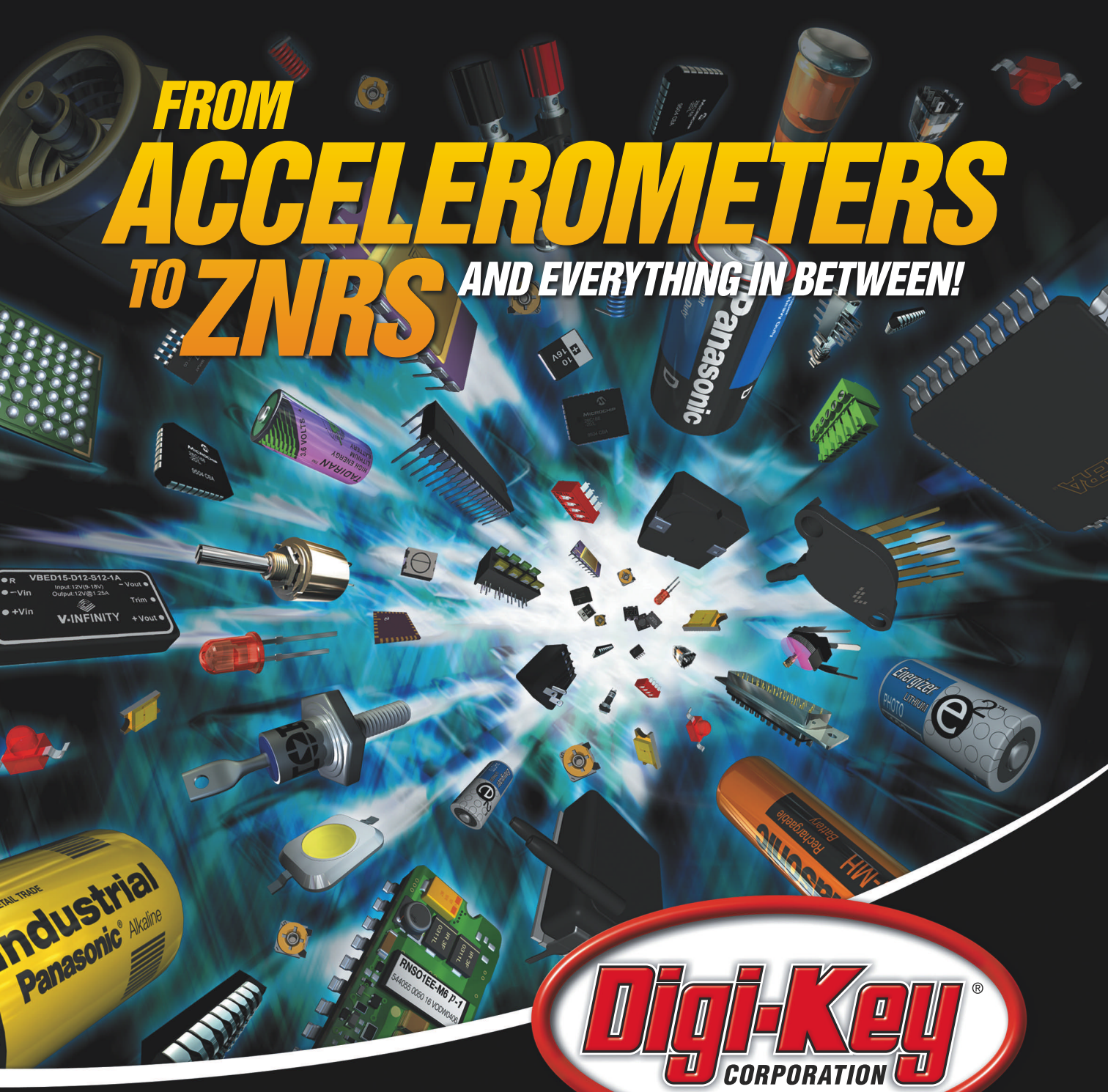

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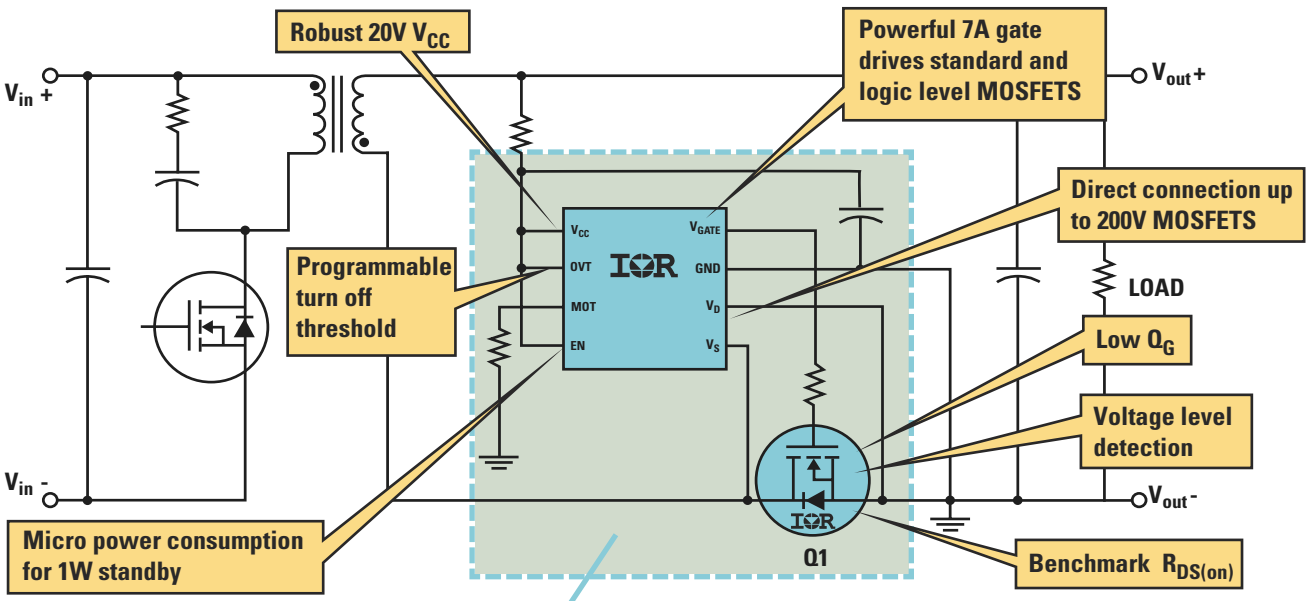

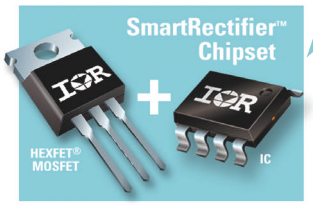

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ICs

Part Number	Package	V_{CC} (V)	V_{FET} (V)	Sw. Freq. Max. (kHz)	Gate Drive	V_{GATE} Clamp (V)	Sleep Current Max. (µA)
IR1167A/SPbF	DIP-8/SO-8	20	<=200	500	+2A/-7A	10.7	200
IR1167B/SPbF	DIP-8/SO-8	20	<=200	500	+2A/-7A	14.5	200
IR1166/SPbF	DIP-8/SO-8	20	<=200	500	+1A/-3.5A	10.7	200

MOSFETS

Part Number	V_{DSS} (V)	$R_{DS(on)}$ max @ 10V (mΩ)	$Q_{G(typ/max)}$ (nC)	Package
IRFB3206PbF	60	3.0	120/170	TO-220
IRFB3207PbF	75	4.1	120/170	TO-220
IRF7853PbF	100	18	28/39	SO-8

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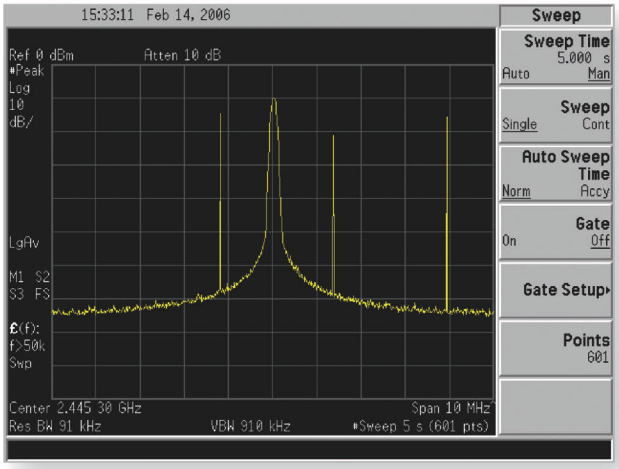
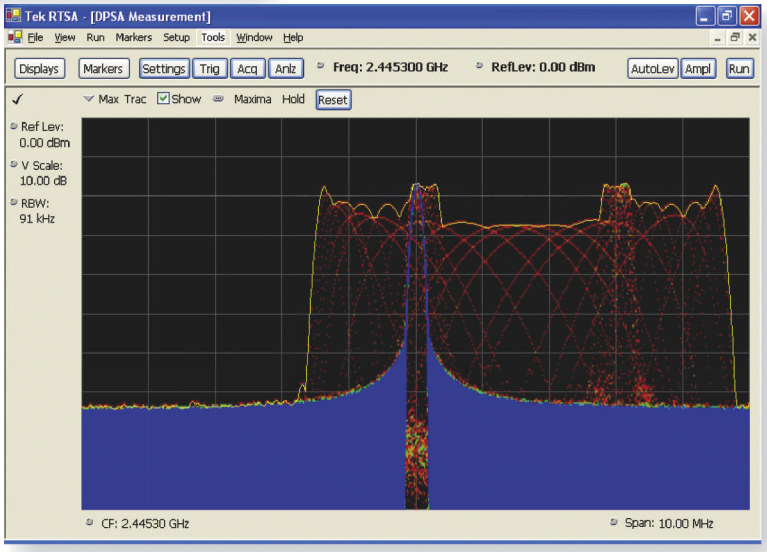


Agilent 5 seconds



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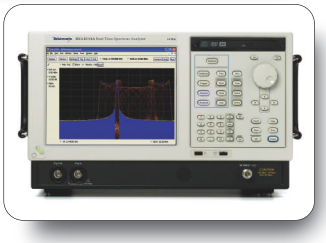

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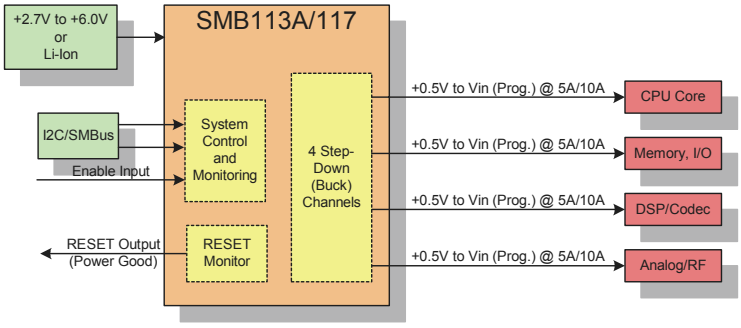

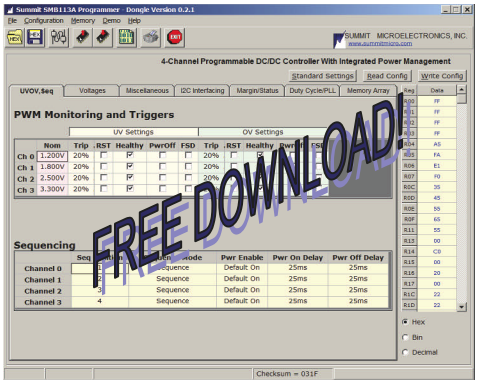

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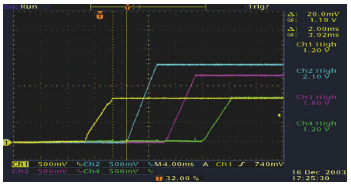
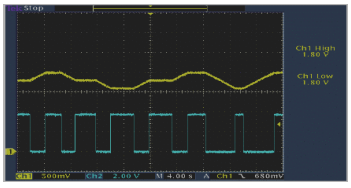


Sequencing



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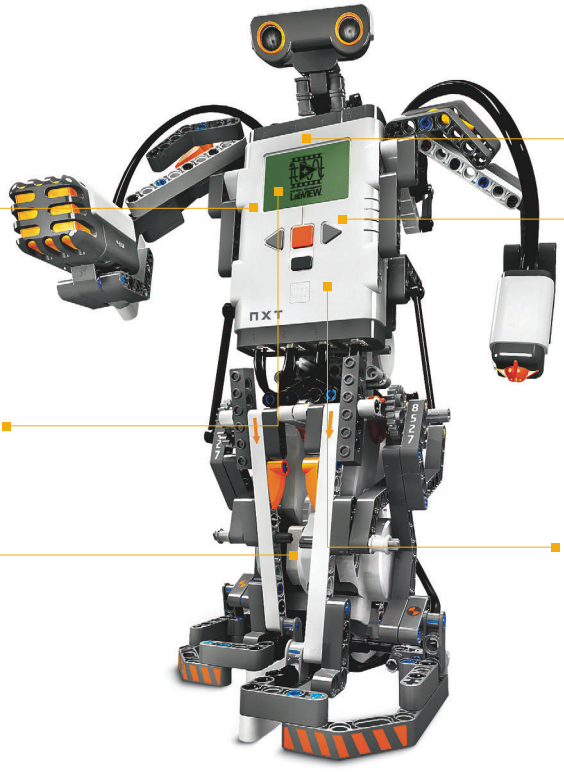

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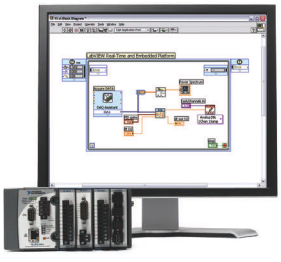

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by Dean Andersen, St Jude Medical

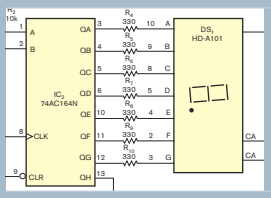
Interface overkill? Is eSATA necessary for your next system design?

by Brian Dipert, Senior Technical Editor

PCI Express prompts quiet evolution

by Richard A Quinnell, Contributing Technical Editor

DESIGNIDEAS



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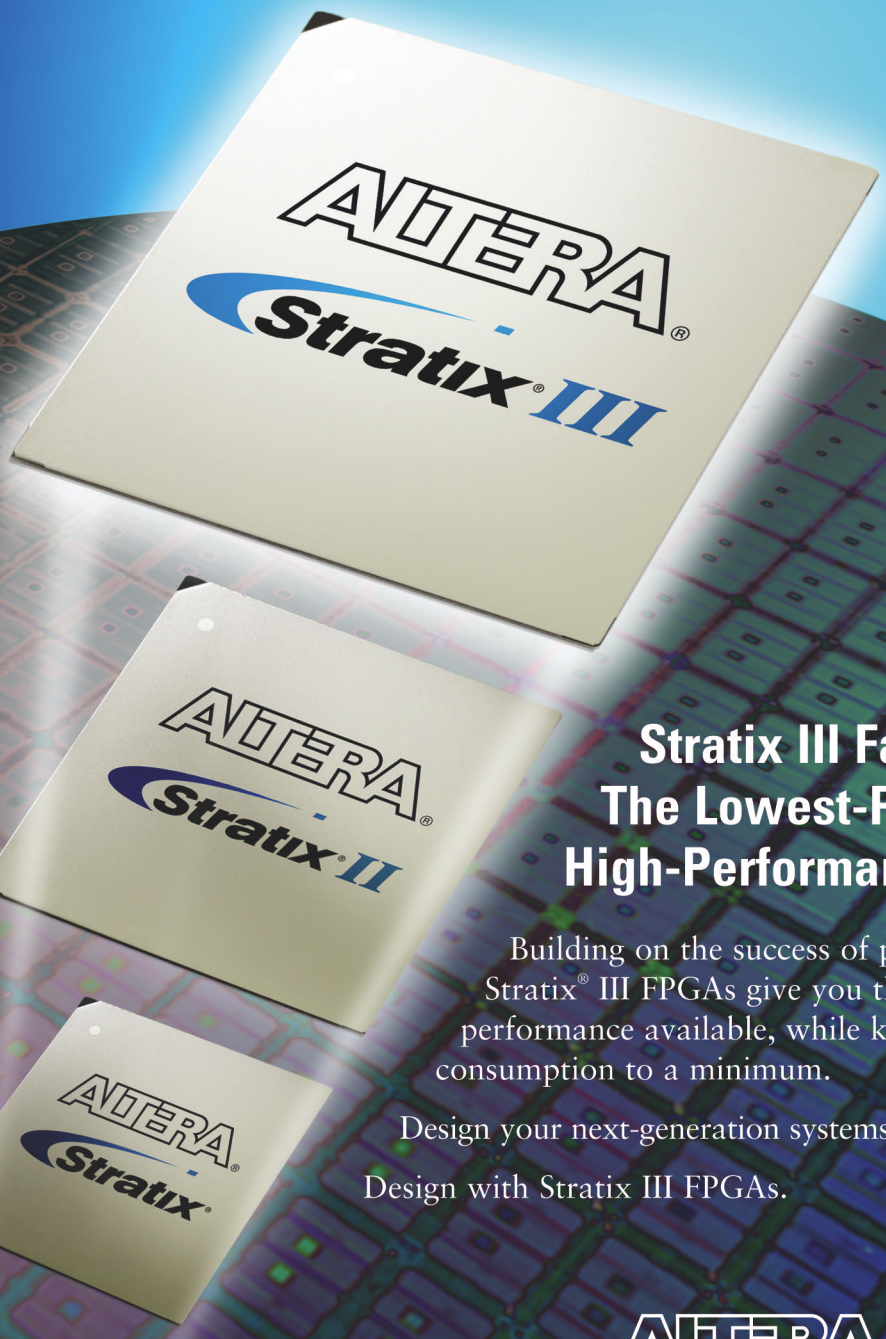

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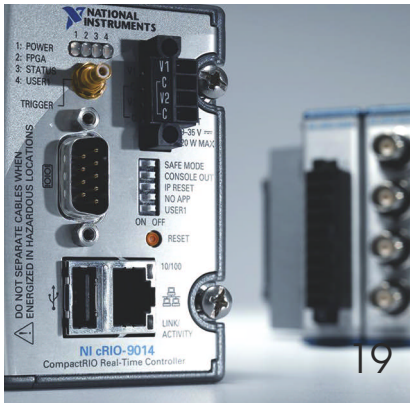

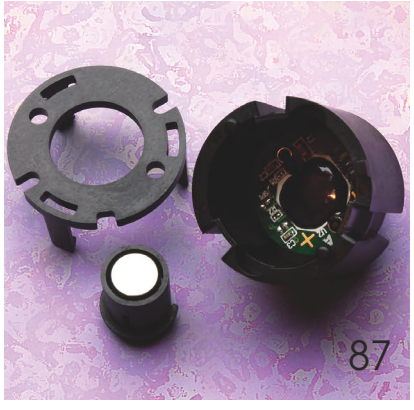

DEPARTMENTS & COLUMNS

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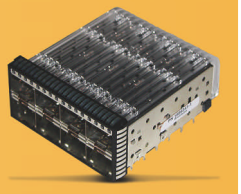

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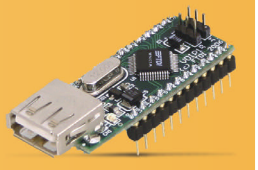

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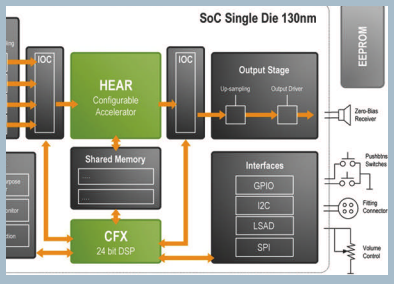

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2007 DSP DIRECTORY

When the 2007 DSP Directory appeared in the April 12 print issue, we hadn't quite put the finishing touches on the dramatically expanded online version (sorry). But we hope you'll agree the online edition was worth waiting for. The directory lets you browse available DSP resources by company or target application, and it includes an enormous amount of data not available in the print edition, including parametric device tables and block diagrams.
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BY MAURY WRIGHT, EDITORIAL DIRECTOR

Draft 802.11n Wi-Fi networks move to mainstream

The tumultuous IEEE 802.11n wireless-LAN-standards process is still months from completion, and the infighting among major players has been worse than in most standards bodies. More than two years ago, Airgo Networks (now part of Qualcomm, www.qualcomm.com) began shipping what some labeled pre-n products (www.edn.com/070510ed1). Now, a host of semiconductor vendors has driven "draft-n-compliant" products to market. I've been negative on both the infighting in the standards body and the premature product announcements. But the draft-n products do deliver improved data rates and range. Moreover, it appears that, in this case, the Wi-Fi Alliance (www.wi-fi.com) certification of products coming in June may be more important than the work of the 802.11n committee.

"I believe it's the Wi-Fi logo that gives consumers confidence," says Bill Bunch, director of product management for wireless LANs at Broadcom. He is correct that consumers want products that interoperate. Bunch claims that users will be able to upgrade all of the products Broadcom has shipped with the draft-n label to the ultimate standard and that they will comply with the Wi-Fi Alliance certification process.

Broadcom currently leads in draft-n IC shipments—a bit ironic given that it was a latecomer to what became the EWC (Enhanced Wireless Consortium), which Intel (www.intel.com) and Atheros (www.atheros.com) formed to speed the technology to market (see "80211n progress: consensus building or end run?" *EDN*, Jan 5, 2006, pg 14, www.edn.com/article/CA6294163). You can believe the Intel and Atheros spin that they were working in the best interest of the industry in accelerating the deployment of new technology or that they were trying to gain an advantage by defining the technology in their own way. In either case, Broadcom had been at odds with that duo before joining the EWC.

As a user and observer, I'm eager for the technology to hit the market. The new network will enable cool applications, such as video distribution, and even drive demand for more bits from the core networks. For almost two years, I've enjoyed the speed and range advantages of several Airgo-based products. Those products have been 802.11g extenders because they interoperate with products from other vendors based on backward compatibility with 802.11g and even 802.11b. The Wi-Fi-certified draft-n products should offer interoperability among vendors with the greater data rates that the new standard offers.

Still, I have some concerns about the draft-n technology and, for that matter, about products that meet the final standard, which are due to debut late this year. All of the 802.11 wireless standards have had options. Manufacturers have been able to skip support of some features to cut costs. The 802.11n technology will be the worst yet. Unlike previous standards, 802.11n defines operation in both the 2.4- and the 5-GHz frequency bands. But the standard does not require manufacturers to implement support for both bands, and most of the draft-n products that vendors are now shipping to consumers support only 2.4-GHz operation.

The 2.4-GHz band has so far served us well, but it's increasingly crowded. Apple (www.apple.com) supports both bands in the draft-n implementation in the company's new Apple TV. As Broadcom's Bunch points out, the 5-GHz band provides 24 additional nonoverlapping channels, whereas the 2.4-GHz band supports only three such channels. Apple likely wanted to ensure that the TV product would find a channel without interference from other Wi-Fi traffic or other products, such as cordless phones.

Bunch claims that Dell (www.dell.com), Acer (www.acer.com), Lenovo (www.lenovo.com), Apple, and Hewlett-Packard (www.hp.com) have all designed notebooks with 5-GHz-capable 802.11n implementations. For now, however, you won't likely find an access point that supports the 5-GHz band. So, even if you have a spiffy, new, 5-GHz-capable notebook and a similarly capable Apple TV, your access point may prohibit operation in the higher band.

Bunch believes that situation will change as the technology matures and costs come down. He points out that dual-band support in a client is much easier and less expensive than dual-band support in an access point. In a client, only one radio operates at any given time. An access point must simultaneously support both bands. All of these scenarios make perfect sense except to the consumer who brings home a bag of Wi-Fi-certified products yet can't take full advantage of the technology. EDN

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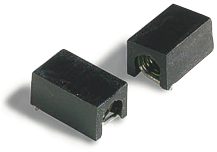
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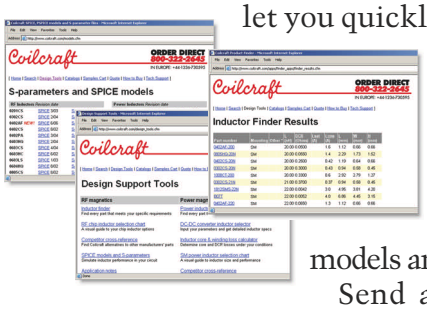

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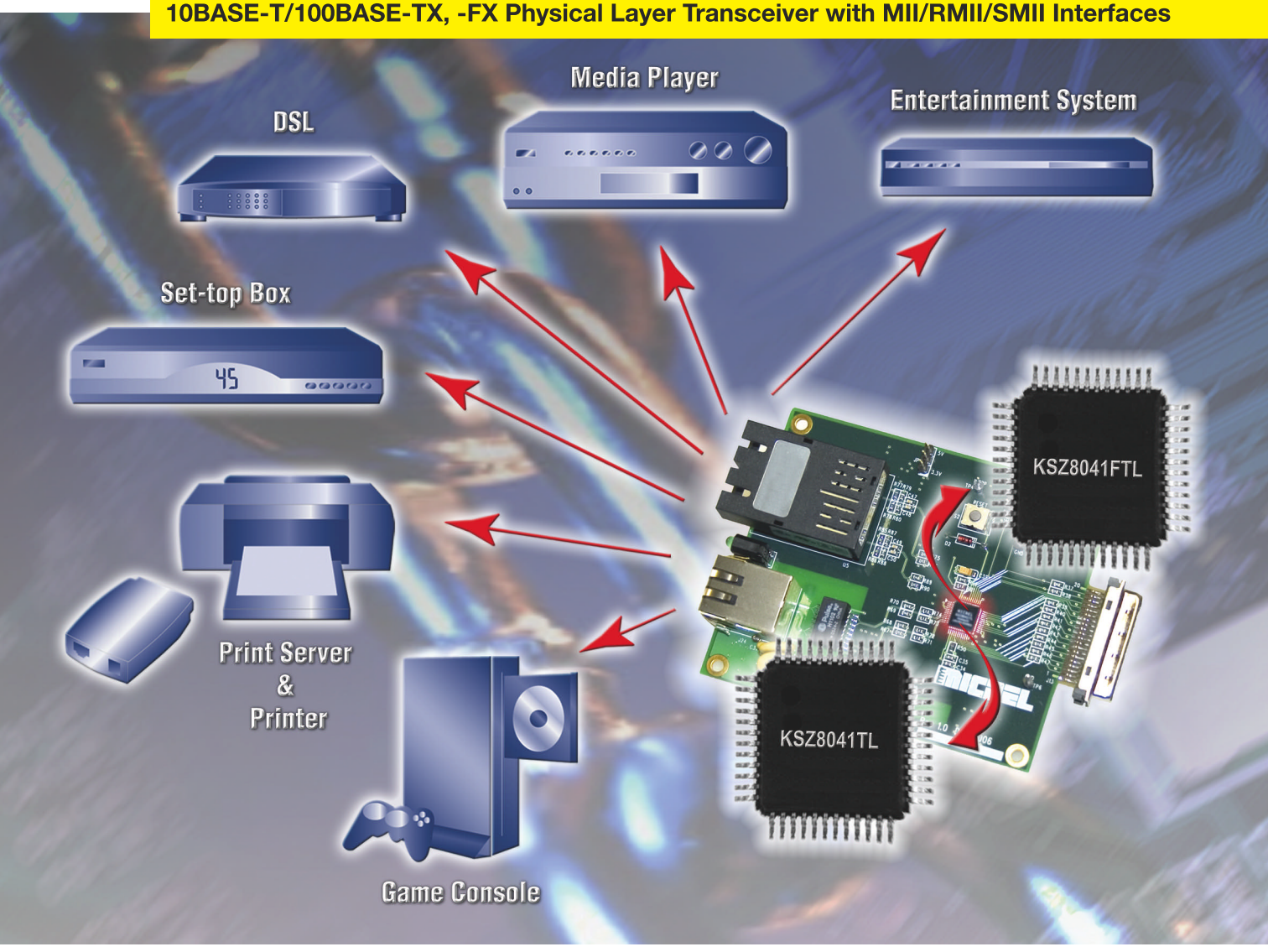

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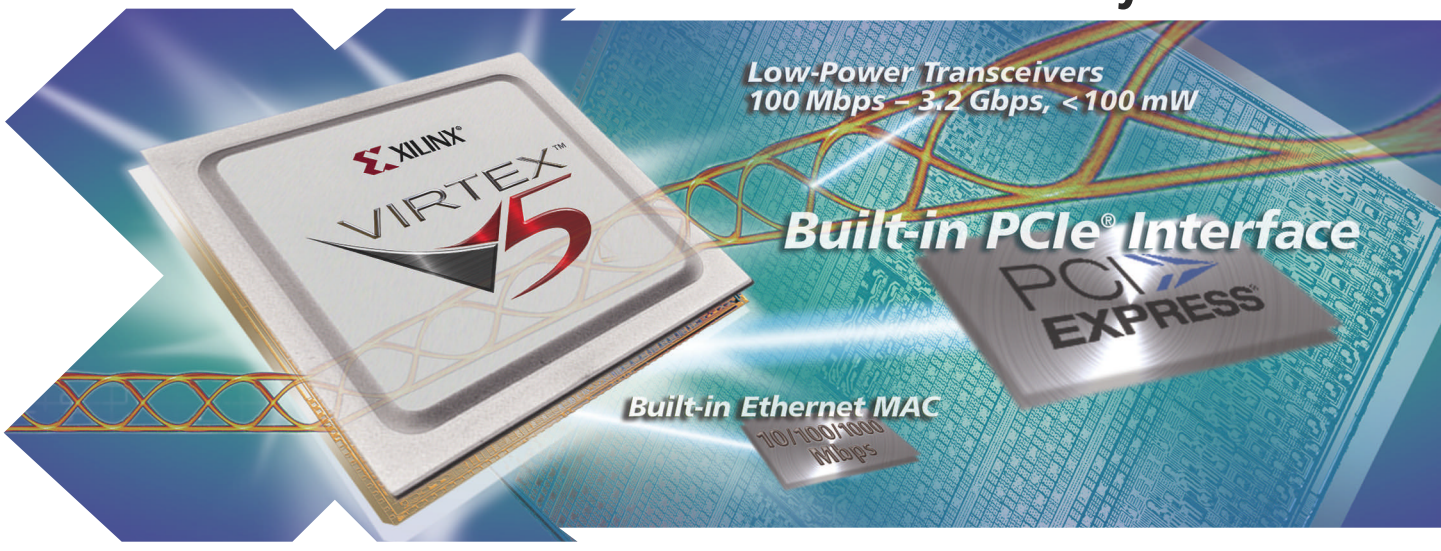

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INNOVATIONS & INNOVATORS

Fanless PC/104-Plus computer runs cool and quiet

Targeting space- and power-limited embedded designs in the industrial, security, transportation, communications, military, and information-appliance markets, WinSystems recently introduced the PPM-GX single-board computer in the PC/104-Plus form factor. The board integrates the CPU, video, Ethernet, USB, COM, LPT, mouse, audio, and keyboard controllers onto a single 3.6×3.8-in. module. The company based the PPM-GX on the 500-MHz, low-power AMD (www.amd.com) GX500@1W processor, and it operates throughout the temperature range of −40 to +85°C without a fan. The Pentium-class GX500@1W CPU runs Windows CE, Windows XP embedded, Linux, and other x86-compatible operating systems, such as VxWorks and QNX.

The low-power, 500-MHz, PPM-GX single-board computer features video, Ethernet, USB, and four COM channels; it operates from −40 to +85°C.

The PPM-GX supports as much as 512 Mbytes of SDRAM and supports both rotational and solid-state disks. The onboard CompactFlash card socket supports devices with capacities as large as 8 Gbytes. The processor features a graphics controller that drives both CRT and flat-panel displays. Along with the typical keyboard/mouse/printer interfaces, the PPM-GX also includes a 10/100 Ethernet controller, four 16C550-compatible UARTs, and two USB ports. The PPM-GX draws typically 1.5A at 5V during normal operation. The unit sells for $495.

—by Warren Webb

▷**WinSystems**, www.winsystems.com.

National Instruments extends embedded controller

National Instruments' latest CompactRIO platform combines a Freescale (www.freescale.com) processor and a Wind River (www.windriver.com) real-time operating system with the built-in Xilinx (www.xilinx.com) FPGA to deliver the extra performance for a variety of embedded- and industrial-system applications, such as high-speed machine control, in-vehicle data logging, and embedded-device prototyping. CompactRIO allows developers to define custom embedded-hardware circuitry using plug-in I/O modules, a reconfigurable FPGA, and LabView graphical-development tools.

The new cRIO-9014 controller combines a 400-MHz Freescale MPC5200 processor with an integrated floating-point unit, a hardware-based memory-management unit, 128 Mbytes of memory, and 2 Gbytes of nonvolatile storage. The VxWorks operating system running on the MPC5200 processor provides the controller with dependable performance to reduce jitter and increase reliability for high-speed-control applications. The cRIO-9014 controller also features a fault-tolerant file system, making it compatible with critical embedded data-logging applications. The price for the the cRIO-9014 CompactRIO starts at $2699, and it is available now.

—by Warren Webb

▷**National Instruments**, www.ni.com.

The new cRIO-9014 CompactRIO controller delivers increased processing speed, memory, and storage for high-performance embedded-control and -monitoring applications.

Mentor pumps up ICE-logic emulation

Mentor Graphics has announced its fifth-generation family of logic emulators, Veloce, which features a new architecture that boasts simulation acceleration and ICE (in-circuit-emulation) performance as fast as 1.5 MHz and features a top capacity of 128 million ASIC gates. Mentor Graphics has been in the emulation business for more than a decade and, during that time, the company has fielded several emulation systems, building some and gaining some from acquisitions of Meta Systems, which offered Celaro, and Ikos, which offered VStation.

The new Veloce, says Eric Selosse, vice president and general manager of Mentor's Emulation Division, is the amalgamation of the best of all those technologies. It features the company's emulation-on-chip technology and builds on the virtual-wires technology that Ikos introduced half a decade ago to speed performance of its VStation emulation systems.

Emulation systems typically comprise either a bunch of linked FPGAs or custom programmable ASICs. Traditionally, FPGA-based systems have been easier for EDA companies to design but didn't offer the performance of custom programmable-ASIC-based systems, such as the one Meta Systems offered in its Celaro emulators. But, in the 1990s, Ikos devised an algorithm to streamline the interconnect and thus the communication of the various FPGAs in the VStation. "You can look at Veloce as a hybrid between what we had in VStation and what we had in Celaro," says Sanjay Sawant, director of marketing for Mentor's Emulation Division. With Veloce, Mentor has incorporated the Ikos virtual-wires technology, but, instead of interconnecting off-the-shelf FPGAs, Mentor uses it to speed the interconnect within and between the custom emulation-on-chip programmable SOCs (systems on chips) Mentor designed for the system. The result is a high-performance emulation system to help designers debug and verify large designs.

"From the VStation family, we have the fast runtime, the ability to handle both synchronous- and asynchronous-design styles, a model footprint, and transaction-based acceleration," says Sawant. "From the Celaro family, we gain the full custom acceleration, fast compilation, and fast debugging." Each emulation-on-chip SOC in Veloce can hold 500,000 gates of equivalent, reconfigurable macro elements. Mentor implemented the SOCs in a 90-nm, eight-layer-copper process.

As for ease of use, the state of the art in logic emulation is for vendors to offer emulation with identical GUIs (graphical user interfaces) and debugging capabilities to those of their simulators and to offer multimode operation. Veloce systems have the same user interface as Mentor's Questa/ModelSim simulation environments and can handle transaction-based simulation/emulation. Whereas the VStation took roughly four hours to complete a full compilation—that is, to program ASIC logic into the emulator—Veloce does a full compilation in half the time and runs as many as 15 million gates per hour. Mentor also improved the system so that, if users want to add triggers to their designs running on the emulator after initial compilation, they can do so without recompiling the design. Whereas VStation users could do one debugging cycle in eight hours, they can now do three in eight hours. As a result, designers can more quickly program their designs into the emulation system, do emulation runs, debug, recompile, and complete large designs.

Mentor offers Veloce in three configurations. The desktop-sized Solo for both simulation acceleration and ICE accommodates one user and has a 16 million-gate capacity. The rack-mountable Trio 24/48 for simulation acceleration accommodates as many as three users and can handle either 8 million or 16 million gates. The server-sized Quattro simulation-acceleration and ICE system accommodates as many as four users and has a capacity of 128 million gates. Mentor offers Veloce for sale outright or for rental, with rental prices starting at $24,000.

—by Michael Santarini

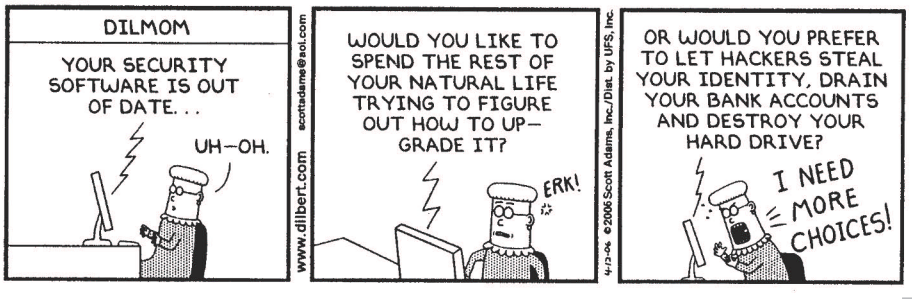
▷**Mentor Graphics**, www.mentor.com.

VELOCE CUSTOMER DEPLOYMENTS

Sample applications*	Gates (millions)	Mode	Performance
Wireless	10	ICE	854 kHz
Set-top box	9	ICE	800 kHz
Chip set	11	ICE	600 kHz
Picture processing	2.8	Stand-alone	1.3 MHz
Voice over Internet Protocol	8	Transaction acceleration	1 MHz
Voice over Internet Protocol	2	Transaction acceleration	1.1 MHz
Wireless	20	Transaction acceleration	775 kHz

*Real-life customer deployments within first six months of life.

DILBERT By Scott Adams



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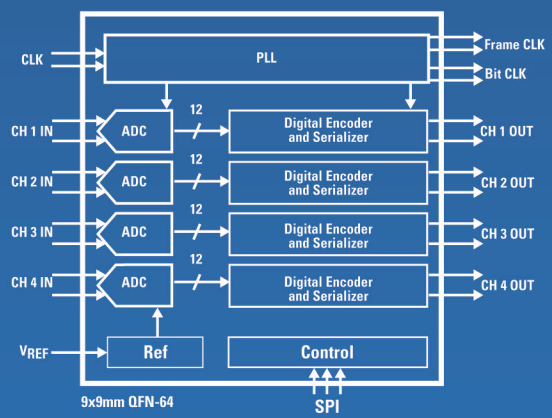
The new **ADS6425** from Texas Instruments is the first in a family of four-channel, low-power, 12- and 14-bit pin-compatible ADCs. Consuming just 410 mW/channel, the 125 MSPS ADS6425 features serialized LVDS outputs that allow four highly programmable ADCs to fit in a small 9x9mm, 64-pin QFN package, making it ideal for a wide variety of high-density, low-power applications.



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Texas Instruments

SST introduces hybrid NAND/NOR All-In-OneMemory

Known primarily for its NOR-memory technology, SST (Silicon Storage Technology) is now adding to its portfolio the All-In-One-Memory device, which mixes NAND, NOR, RAM, and a memory controller in one system-in-package offering. The All-In-OneMemory will go head to head in the market with a slew of other mixed-memory code- and data-storage devices, such as Samsung's (www.samsung.com) OneNAND, SanDisk's (www.sandisk.com) mDoC, and other devices vying for the system-memory slot in the high-end-handheld-device market.

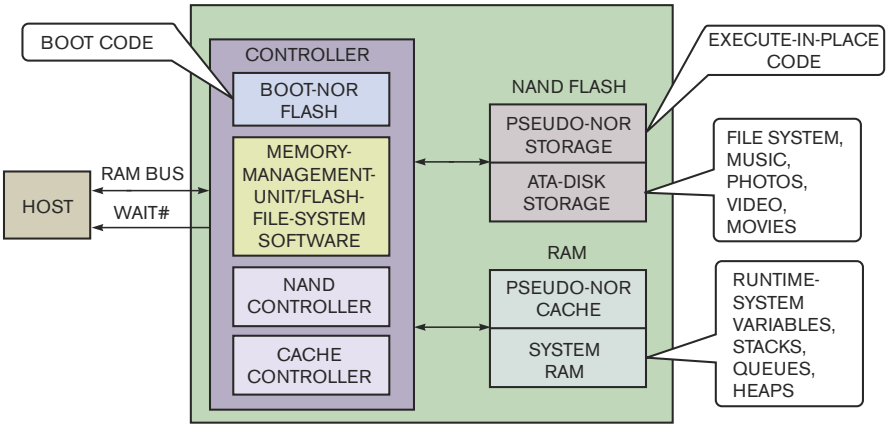
SST expects to introduce the first silicon in the second half of the year and has not yet revealed the densities or nitty-gritty details of its new devices. Frank Lin, vice president of application-specific-controller products at SST, says, however, that each of the new devices in the family will feature a NOR and a NAND that an SST-built memory controller manages. The controller seemingly is the key innovation of the All-In-OneMemory because it decides which type of memory is best for a task and communicates tasks to the off-chip host CPU through a RAM bus. The controller includes embedded SuperFlash NOR blocks for boot code, a flash-file system for NAND-flash management, and a cache-memory controller for pseudo-NOR that emulates high-density NOR flash.

"The All-In-OneMemory puts the benefits of NOR and the benefits of NAND into one subsystem," says Lin. "We've added a controller to the subsystem, which eliminates the limitations of the NOR and the limitations of the NAND. We now provide a unified storage system for both data and code, and we offer advanced security features because of the controller." The new system features as much as 8 bits of random-ECC (error-correction code) and a cache controller to handle demand paging and reduces the overall RAM requirements for designs.

"We are removing all the hardware and software requirements, [such as] virtual paging, swap in, and swap out, from the host CPU for regular memory management, and we also removed the flash-file system and the ECC hardware for the NAND controller from the host controller," Lin says. "The memory controller also optimizes the use of the NAND and NOR memories."

All-In-OneMemory's map, the host CPU, will interface with four random-access blocks and one sequential-access block through a single bus. The random-access blocks consist of a memory-controller-embedded SuperFlash NOR block for instant-on boot-up of the system, a high-speed pseudo-NOR on a separate NAND for executing time-critical code and data, a pseudo-NOR on the NAND for code and data storage, and a RAM block for working code and data and pseudo-NOR caching. The sequential-access block comprises an ATA data-storage block on the NAND for non-XIP (execute-in-place) code and data. SST currently has working silicon for the device and expects to have the device ready in volume in the second half of this year.**—by Michael Santarini**

▷**Silicon Storage Technology**, www.sst.com.

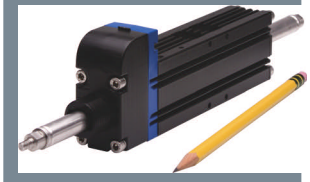


SST's All-In-OneMemory features a memory-controller NAND device and RAM in a system in package.

05.10.07

DIRECT-DRIVE LINEAR ACTUATOR MAKES FAST, PRECISE MOVEMENTS

Traditional lead-screw and belt-drive positioners have relatively large moving parts, making fine repetitive motion difficult. They also suffer from high wear and tear due to friction, making them wear out more quickly. In contrast, linear actuators, such as Copley Controls new STA11 direct-drive device, are lighter and have minimal friction, making them well-suited for applications requiring fast, repetitive, millimeter-long excursions.



Linear actuators are alternatives to traditional positioners, such as lead-screw and belt-drive motors.

The STA11 provides 14- to 232-mm strokes, ±12-micron repeatability, and 10 million operating cycles. Peak force and velocity are 92N and 4.7m/sec. A multiactuator assembly with 10 actuators measures less than 12 in. wide. The forcer has lubrication-free bearings to support the thrust rod, and the unit has the same form factor as regular pneumatic and electric actuators. The STA11 sells for $793, including cable.—by Margery Conner

▶**Copley Controls Corp, www.copleycontrols.com.**

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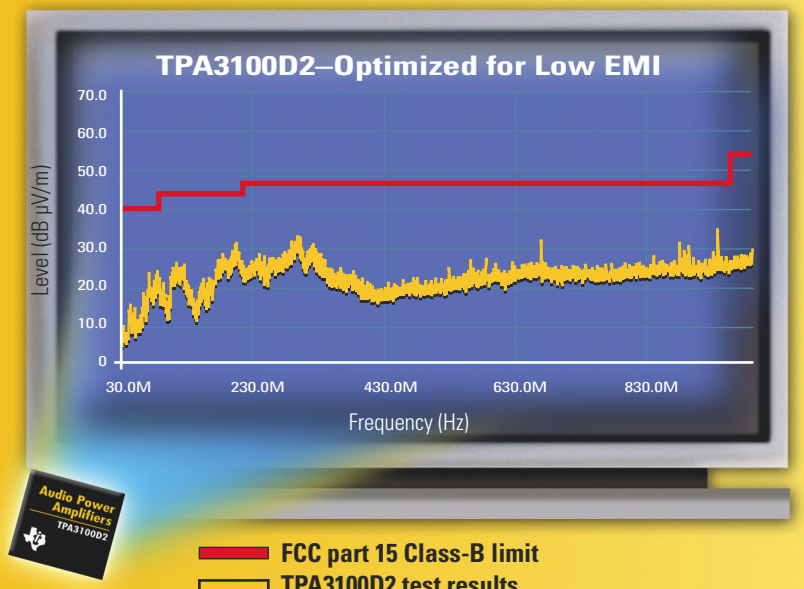

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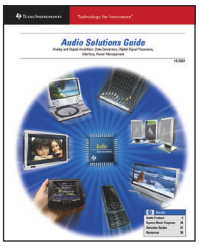

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TEXAS INSTRUMENTS

Xilinx adds power supply, thermal monitor to Virtex-5 FPGAs

To help users of its 65-nm Virtex-5 FGPAs get a better handle on on-chip thermal- and power-management issues, Xilinx recently released its System Monitor tool. The tool will allow users to obtain power and thermal information directly from the JTAG test port on Virtex devices without making elaborate connections. The tool has access to an ADC on the Virtex chip. "Now, you read out a digital word [through the JTAG port] and get a representation of the die temperature, especially for power supplies," says Anthony Collins, staff marketing engineer for mixed-signal products in the company's Advanced Products Group.

Until now, Xilinx users could monitor on-chip thermal and supply voltage only through a thermal diode on Virtex devices. "It allowed customers to hook up external monitoring circuitry to a thermal diode on our die as a way of figuring out what the die temperature was for any given design," Collins says. "Some customers have been successful using the diode, and others have not."

> If there is any over-temperature condition or power-supply issue, you can switch to redundant hardware.

The diode represented about 10% of what engineers need for monitoring the temperature, according to Collins. "You still needed to do a fair amount of engineering work with an external IC or PCB [printed-circuit-board] design," he says. "And some of those implementations are sensitive to noise. It really depended on the experience of the designer how substantially that diode monitor was implemented."

The System Monitor relies on a 10-bit, 200k-sample/sec ADC and includes automatic-calibration and self-checking features to monitor the IC over a temperature range of −40 to +125°C, Collins says. Xilinx intends for the System Monitor to satisfy two use models. First, the system should help designers with development test and debugging. The tool will help users create power supplies or perform overall thermal management. "You can now read back temperature and power-supply information through the same JTAG output, or you can enable a number of analog inputs and read other analog quantities via JTAG, as well," he says. "So, we allow you to monitor other analog quantities on the PCB, not just the FPGA temperature and voltages."

Second, the system will help users monitor and manage thermal issues in the FPGA after they have deployed the system in the field. Collins says that a number of standards are evolving that describe the requirements for monitoring the physical environment inside a box or chassis. Most of these standards aim to manage redundancy within the box. With System Monitor, Xilinx allows customers to use some of the programmable logic to customize the System Monitor block so that they can easily integrate it into the system-management infrastructure. They can add an I^2C interface or an Ethernet channel to the System Monitor. After deployment of the system, users can gather power-supply and temperature data to ensure that the box remains reliable. "If there is any overtemperature condition or power-supply issue, such as drift, you can switch over to redundant hardware," he says. Xilinx will include System Monitor free in the latest update of its ISE 9.1i FPGA programming suite. Users can access the System Monitor features with the new System Monitor Wizard in that update.

—by Michael Santarini

▷**Xilinx**, www.xilinx.com.

FEEDBACK LOOP

"We took the equipment back to the lab and found the source of the problem: Most of the parts had fallen off the board as the solder had melted, and things were 'lightly toasted' inside. Having nothing to lose, we soldered them back on again and applied power; oddly enough, the circuitry still functioned, although very much noisier than when first installed and with very large offsets."

—Bob T, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6426879. Add your comments.

TOTALVIEW OFFERS MULTICORE-DEBUGGING FRAMEWORK

Etnus changed its name to TotalView Technologies last month at the Embedded Systems Conference in San Jose, CA, as it announced a multicore-debugging framework. The framework comprises components addressing the source code, memory, performance, data-centric views, and active Web support. The TotalView debugger supports Linux, Unix, and Macintosh OS X targets and can scale to accommodate debugging of thousands of cores. The latest version of TotalView includes new features, such as enhanced breakpoint-setting capabilities, the ability to show class-static variable data, and rule-definition abilities for source-code searches.

MemoryScape, a focused, interactive memory debugger, helps designers understand how their programs are using memory and subsequently identifies and resolves problems, such as memory leaks and heap-allocation overwrites. MemoryScape allows developers to monitor memory usage while their applications are running. The performance, data-centric, and active-Web-tool-suite components will be available in the second half of 2007. TotalView is now available in a variety of flexible licensing configurations, including individual, enterprise, team, team plus, and rental. It is available with and without memory debugging.—by Robert Cravotta

▶**TotalView, www.totalviewtech.com.**

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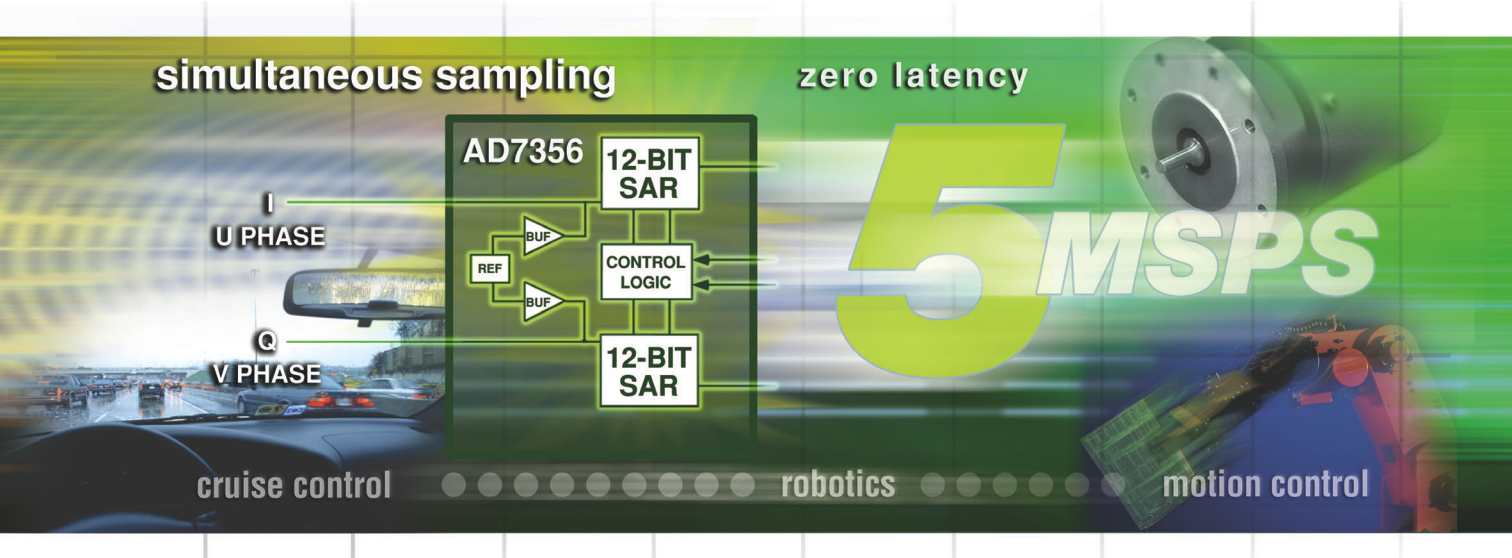

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VOICES

Marvell's Nikhil Balram: a "visual-pipeline" view

Nikhil Balram is vice president and general manager of the digital-entertainment business unit of the communications-and-consumer-business group at Marvell (www.marvell.com). Previously the chief technology officer for National Semiconductor's displays group, he most recently served as the general manager of the company's high-definition-products division. Balram holds bachelor's, master's, and doctorate degrees in electrical engineering from Carnegie-Mellon University (Pittsburgh). *EDN* recently asked his opinions on the state of video processing, displays, media distribution, and more. The following is a small sampling of those opinions. For more, go to www.edn.com/070510voices.

You've certainly had an interesting career so far. Are there any valuable lessons you've learned?

A As evident in my career history, I like to take a system, or 'pipeline,' point of view. From a technical perspective as an imaging/video/display engineer, this [viewpoint] means understanding the whole 'visual pipeline' from pixel creation to pixel rendering. Applying the same mindset as a consumer-electronics professional means understanding the product pipeline—from algorithm and feature invention to silicon and software creation to design of the system product, all the way to the sale and how the consumer uses the product.

To what degree do you think that semiconductor vendors' integration-cultivated price drops created the mass market for video processing, versus the other way around? In other words, which came first: the customer demand or the product supply?

A This one is easy. The chicken came first. Seriously … for semiconductors, the end product (system) usually comes first and establishes itself as a desirable consumer product, and this [occurrence] motivates semiconductor companies to invest in improvements in quality, feature set, and cost. Once they start to invest, it starts a strong self-reinforcing positive cycle, which gives the impression of the chicken and the egg. But, if you go back to the beginning, the starting point is always the chicken.

A fundamental tension in the semiconductor industry is the tug of war between what you do in hardware versus what you do in software. What are your thoughts?

A This is a basic question that plays out in every major market but whose answers are very predictable. Periodically, we have companies that insist on applying the answer that fits their strength or their preferred business model to every market they enter. But if their preferred answer is at odds with the most fundamental aspect of the market, they fail. The fundamental aspect I am referring to is the need for flexibility.

How do you see the current situation as well as the future of displays?

A I think we all know about the rapid decline of CRTs. Comparing LCDs to plasma from a technology-characteristic perspective has its merits. When people ask me for a recommendation, I always ask about how they plan to use it. For dark-home-theater viewing, an emissive display that produces real black is preferred, while, in a bright setting, the high light output possible with transmissive displays is preferable. So, I recommend plasma for home-theater-like viewing and LCD for bright-room multiuse. Why not one of each?

Displays are meaningless without content to display on them. What do you think the potential is for widespread ascendancy of high-definition optical discs versus the current champion, DVD?

A I think good, crisp marketing of blue-laser HD media in conjunction with marketing of 1080p displays can start a self-reinforcing virtuous cycle with consumers. Blue laser got off to a rocky start last year with the format war and less-than-perfect product launches. But things look much more promising this year. I am already hearing that, in Europe, the promise of HD-optical media is a major driver for the adoption of 'HD-ready' TVs, since the road map for broadcast of HD is still fragmented and uncertain. My key rule of thumb for whether something will be successful in the consumer market is: Can the benefit be shown in a convincing manner to the average consumer?

Some prognosticators claim that the mind- and market-share battle between Blu-ray and HD DVD is irrelevant—that purchased or rented Internet-downloadable movies will obsolete them both before they have the chance to establish any tangible long-term beachhead. What do you think?

A I don't think these [technologies] will be mutually exclusive. A lot of money is made by efficiently managing the rollout of professionally created entertainment content—starting with the theatrical release, moving to the hotel/cable pay-per-view release, then the airline release, then the release to DVD, and, finally, the broadcast release. I believe these windows will continue to drive sales and rentals of the most popular content in the form of packaged optical media for the growing audience with great home-theater setups.

—by Brian Dipert

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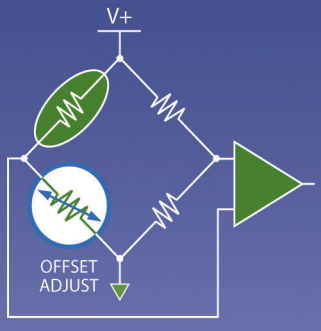
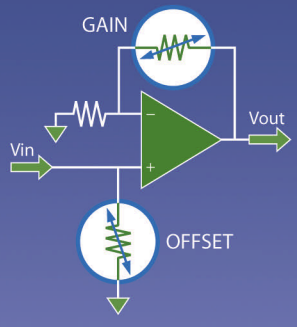
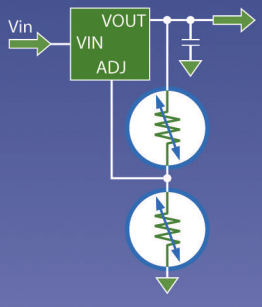


Sensor Compensation



Amplifier Calibration



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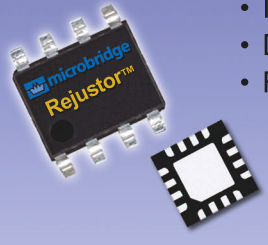

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MBD-153-AL	1:1	10.5K - 15K	10.5K - 15K
MBD-333-AL	1:1	23K - 33K	23K - 33K
MBD-153-KL	1:3	10.5K - 15K	31.5K - 45K
MBD-472-CL	1:5	3.3K - 4.7K	16.5K - 23.5K
MBD-902-CL	1:5	6.3K - 9K	31.5K - 45K
MBD-103-XL	1:7	7K - 10K	49K - 70K

Standard Product - Available in QFN or SOIC

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MBD-153-AS	1:1	10.5K - 15K	10.5K - 15K
MBD-472-AS	1:1	3.3K - 4.7K	3.3K - 4.7K
MBD-903-AS	1:1	63K - 90K	63K - 90K
MBD-103-AS	1:1	7K - 10K	7K - 10K
MBD-103-BS	1:2	7K - 10K	14K - 20K
MBD-103-CS	1:5	7K - 10K	35K - 50K
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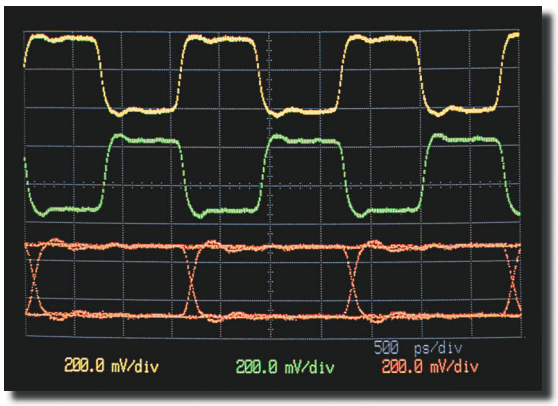

Plot shows complementary clocks and PRBS (opt. 01) outputs at 622.08 Mb/s with LVDS levels. Traces have transition times of 80 ps and jitter less than 1 ps (rms).

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BY BONNIE BAKER

Analog versus digital: riding the fence

As an analog-world descendant, I always hear comments in the hallway about how digital designers don't really understand analog issues. Digital designers will go so far as to unsympathetically say the same about analog-IC designers. There is no bridge between these two camps unless the participants ride the fence and enter the mixed-signal domain together.

True to the analog spirit, not all data converters use the same digital format. Some converters use unsigned-binary-data types; other converters use two's-complement signed data. To even further complicate matters, some converters produce 12- or 14-bit output words, and others produce 16-bit output words. Yet another technology is the 24-bit delta-sigma converter.

Forget the reasons for these analog-design decisions. With all of these converters, the location of the ADC LSB is in the processor's 0-bit location within the 8-, 16-, or 32-bit word. This situation makes perfect sense to an analog designer. However, the signed-bit of a 12-bit converter resides in position 11 in the processor. If you assign a 16-bit-wide C variable to the converter's output word, C assumes that the sign bit is in position 15. The processor does not recognize a negative number from the converter and assumes that all codes from the 12-bit, bipolar-in ADC are positive. This situation occurs because the signed bit is in the wrong position.

You can approach this problem in several ways. The first, a read-modify-write approach, shifts data in the processor register. The CPU reads the data, shifts the bits in the register containing the data by the necessary amount of bit positions, and writes the data back to memory. A DSP can complete this shift with one cycle. A controller requires many cycles for this shift process. If this strategy is the one you choose, be careful of cache incoherency. Cache incoherency means that the cache is unaware that the DMA controller has placed new words in memory. As a result, the CPU instead shifts the old contents of the cache. It is important to remember that whenever you implement a bit shift to the left, you multiply the ADC results by two.

Another option is to shift the data into the right position in a processor loop. On the downside, this approach uses the CPU and requires additional MIPS. Another alternative is to directly connect the converter to the processor's data bus. If you connect bit 11 of the 12-bit converter to bit 15 of the processor's data bus, the sign bit will then be in the right place. Complete the data-acquisition task by zeroing register bits 11 through 14. Otherwise, these bits are indeterminate. This approach is possible only with parallel interfaces. In this scenario, the DMA-based transfer need not shift data later on.

Serial-port users are more fortunate than parallel-port users because most of the serial ports in processors offer the receiving feature of "left justify and zero fill LSBs" or "right justify and sign-extend MSBs." This feature significantly reduces the amount of work the CPU must perform once the data is in memory, with one drawback. Some serial ports work only if the received word length is a power of two, such as a 16-bit word length. This receiving feature does not work with 12-, 14-, or 24-bit values.

Analog designers can help with the processor-interface problem. All the processors I know about have 8-, 16- or 32-bit data types, but I have never heard of a 12- or 14-bit data type. Until all of the analog-chip designers take the leap and straddle the fence, don't take things for granted when you are designing the digital interface to a converter. Read the ADC data sheet and verify the bit positions in the transmission across the digital interface. If you do this initial examination of the ADC's documented digital interface, you will be more successful with your first spin on the design. EDN

Special thanks to my digital buddy, Richard Oed, systems engineer with the data-acquisition-products group at Texas Instruments.

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1 Oed, Richard, "Let's Talk! Ten things to remember if your data converter is to understand what a DSP is saying to it," *New Electronics*, March 2005, http://direct.bl.uk/bld/PlaceOrder.do?UIN=164814814&ETOC=RN&from=searchengine.

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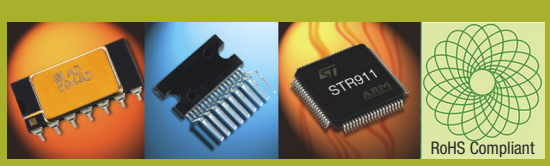

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BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Power and ground design

System-level power-supply design has always been challenging. The continual shrinking of IC-process geometries has generated a major increase in mixed-voltage and -mode SOCs (systems on chips). This development, in turn, has spawned a number of new software tools for assisting engineers in this design effort. These tools fall into two main categories: supply feed/drop and noise.

At the IC level, other approaches to the power-supply feed/drop problem are IR drop and electromigration analysis. The main challenges for IR and electromigration issues are simply accommodating the large lines in the space available, and the ability to deliver the necessary voltage and current to supply the active circuitry. In addition to addressing the size of the lines to minimize voltage drop, the size of the vias connecting the lines is critical to ensuring that the peak current can pass from layer to layer where necessary. Both these physical-manufacturing rules and their associated interlayer-design rules have systematic-analysis options that academia developed and then successfully implemented into commercial EDA tools. This design step has gone from being a manual task to being an automated-analysis task. Now, some SOC and board-level physical-design tools offer automated implementation with analysis.

The noise problem includes supply ripple and ground bounce. Supply ripple comprises injected signals that ride on the positive-power-supply rail, the negative-power-supply rails that are not at the system ground, or both. A variety of both automated and manual tools can analyze these signals. Automated tools generally do not quantify the noise. They give simple responses to simple questions, such as "Is the signal in an acceptable window?" In general, the industry does not use place-and-route or postlayout-verification tools but instead uses high-capacity SPICE tools for this task.

Ground bounce is one of the biggest challenges facing DSM (deep-submicron) design. Because ground bounce affects the system's global reference, none of the high-level simulation tools, such as analog/mixed-signal simulators, postlayout-validation tools, and place-and-route tools, can perform the analysis. This issue forces engineers to solve the problem with large input decks for SPICE simulation. SPICE simulation is necessary because of the requirement for analyzing both time- and frequency-domain simulation. This ground noise, which typically occurs through substrate injection and leakage, is especially critical for low-voltage applications with dramatically reduced PSRRs (power-supply-rejection ratios) and SNRs.

Standard mixed-signal designs operating at 3V or higher enjoy handcrafted power grids with wide lines, multiple vias, and interlayer shielding, in addition to guardbands and isolation techniques, all of which result in PSRR levels greater than 100 dB. Most mobile-battery applications require more than 60 dB of PSRR; otherwise, low-power-shutdown situations occur. Cable-interface circuitry, such as USB, HDMI, DVI, or Ethernet, uses differential-signal processing, and, as a result, ground ripple and its frequency composition are key, because the ground acts as a reference for extracting data embedded on a carrier signal.

Most automated power-grid options aim to minimize IR drop without taking into account the associated noise and harmonic performance; thus, they can produce PSRR levels lower than 60 dB. Solving this multivariable set of simultaneous IR-drop and noise conditions as separate and independent linear problems is unrealistic for designs of less than 130 nm or for systems operating at high frequencies or with accuracy of greater than 12 bits. No automated tools other than standard SPICE can perform this analysis. IC and systems designers in the automotive, audio, video, military, and industrial-electronic sectors point to hand layout, SPICE analysis, and a design guru in a dark cube as the main solutions for power-grid sign-off. An example is a system-level design by Creation Audio Labs (www.creationaudiolabs.com), which simultaneously supports both a PSRR and an SNR of greater than 110 dB. Further, the entire design has either a battery or a commercial-grade external power supply and less than 20 mV of IR drop.

For 65-nm and smaller processes, the reduced operating voltages and higher clock/switching frequencies dramatically increase the importance of power-supply sign-off and analysis in the design flow. This factor will drive multithreaded and multiprocessor SPICE tools that support both frequency- and time-domain analysis. EDN

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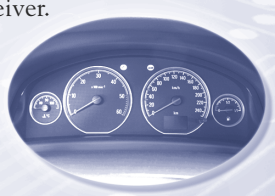

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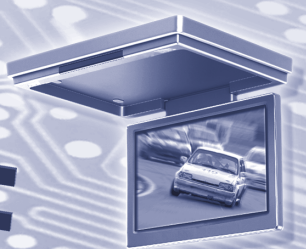

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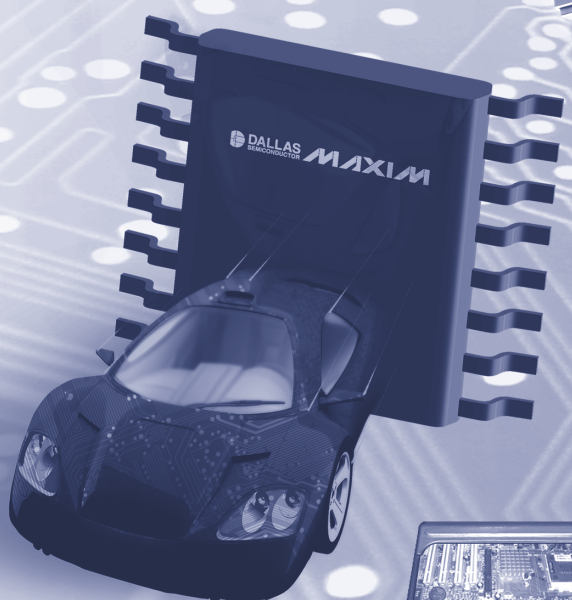

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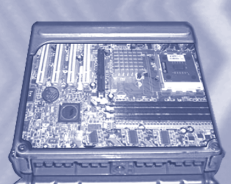

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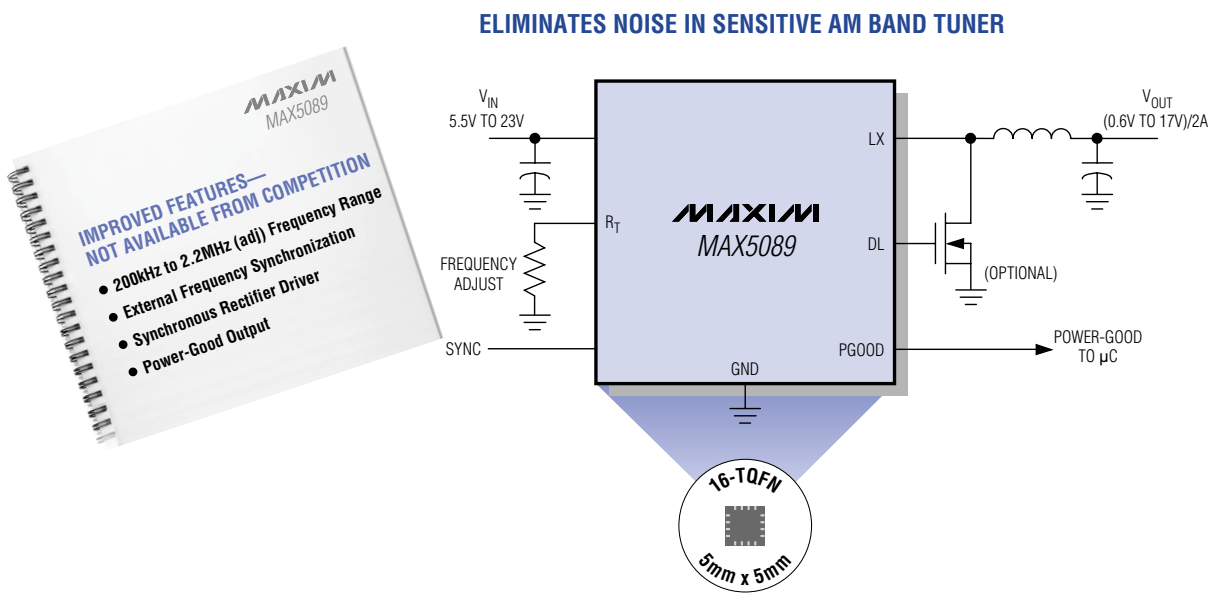

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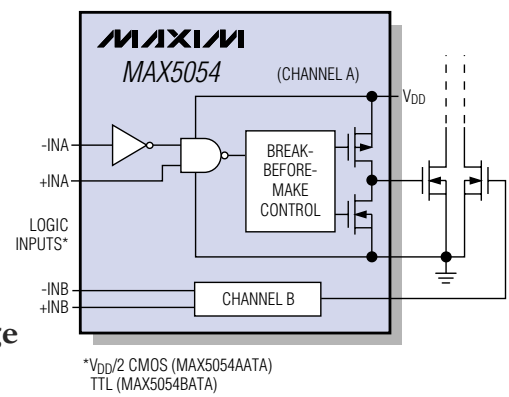

Additional Features

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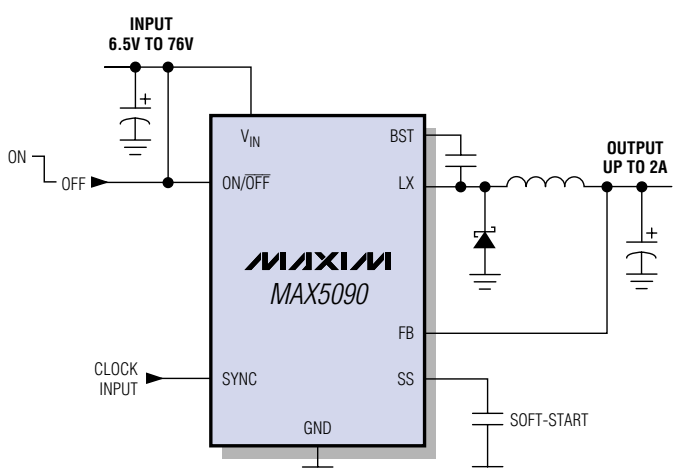

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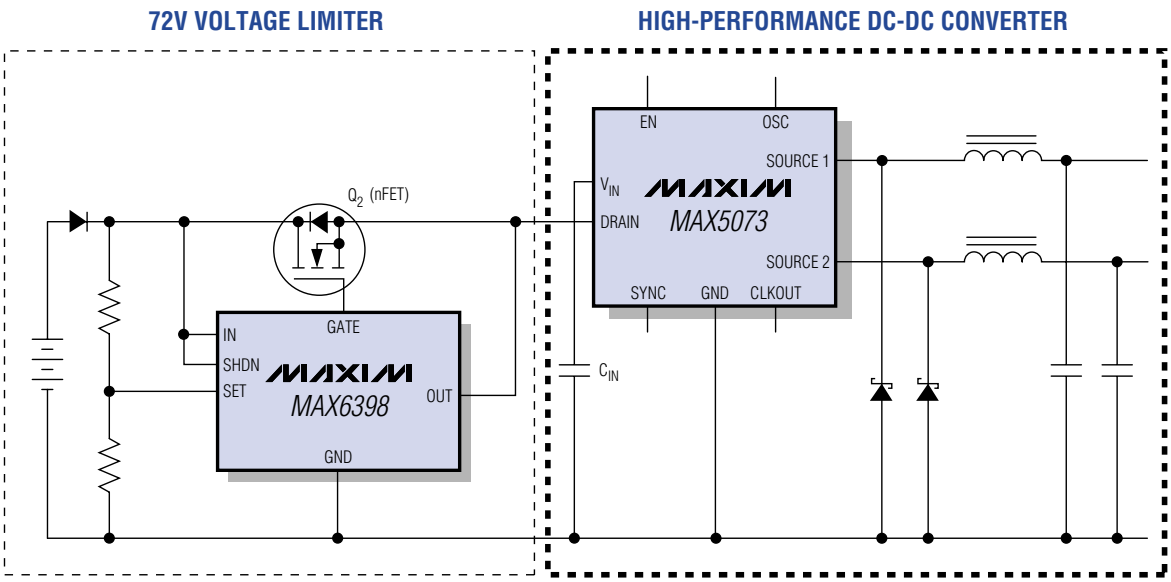
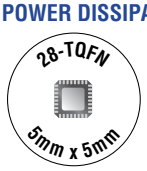


MAX6398 Features

- Load-Dump Protection
  - Up to 72V Wide Supply-Voltage Range
  - Turns Off FET or Limits Voltage During High-Voltage Transients
  - Eliminates the Need for MOVs or TVSs

MAX5073
HIGH POWER DISSIPATION



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  - External Frequency Synchronization
  - 2.2MHz Operation Eliminates Interference in Radio AM Band
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  - Tiny 5mm x 5mm TQFN Dissipates 2.7W of Continuous Power at +70°C
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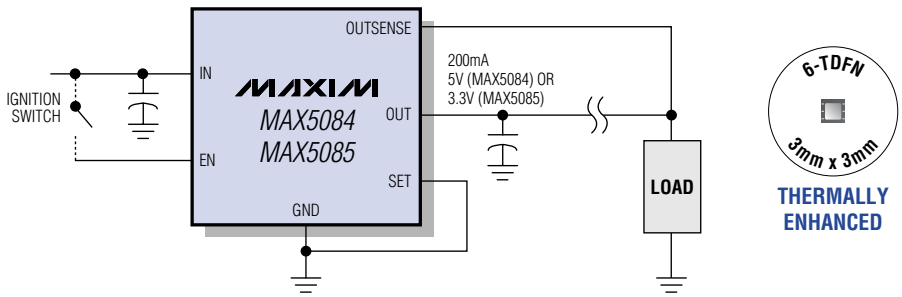


Rugged Design

- Guaranteed Operation over -40°C to +125°C Temperature Range
- Thermal Shutdown and Short-Circuit Current-Limit Protection Up to 65V Input
- Ideal for "Always-On" Supplies in Body Controls and RKE Applications

No MOVs or TVSs Needed

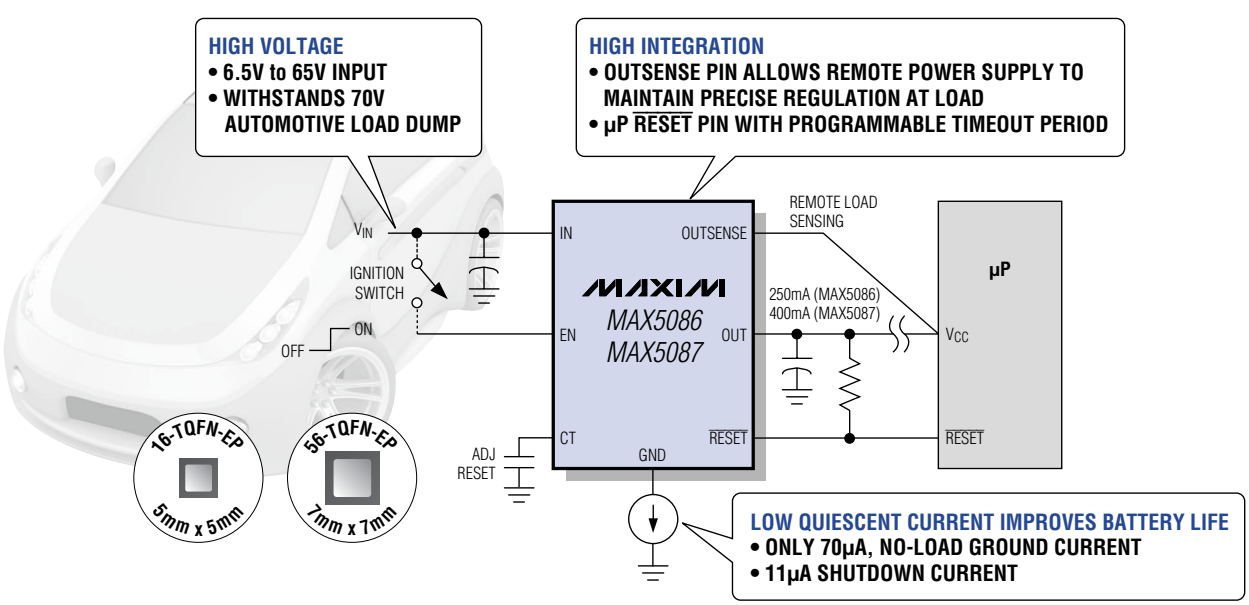
- Wide 6.5V to 65V Input-Voltage Range
- Withstand Up to 80V Automotive Load Dump

High Performance

- OUTSENSE Allows Remote Power Supply to Maintain Precise Regulation at Load
- Under 50µA Quiescent Current at No-Load
- Low 6µA Shutdown Current

65V Input, Low-I_Q Linear Regulators Now in Tiny TQFN Packages

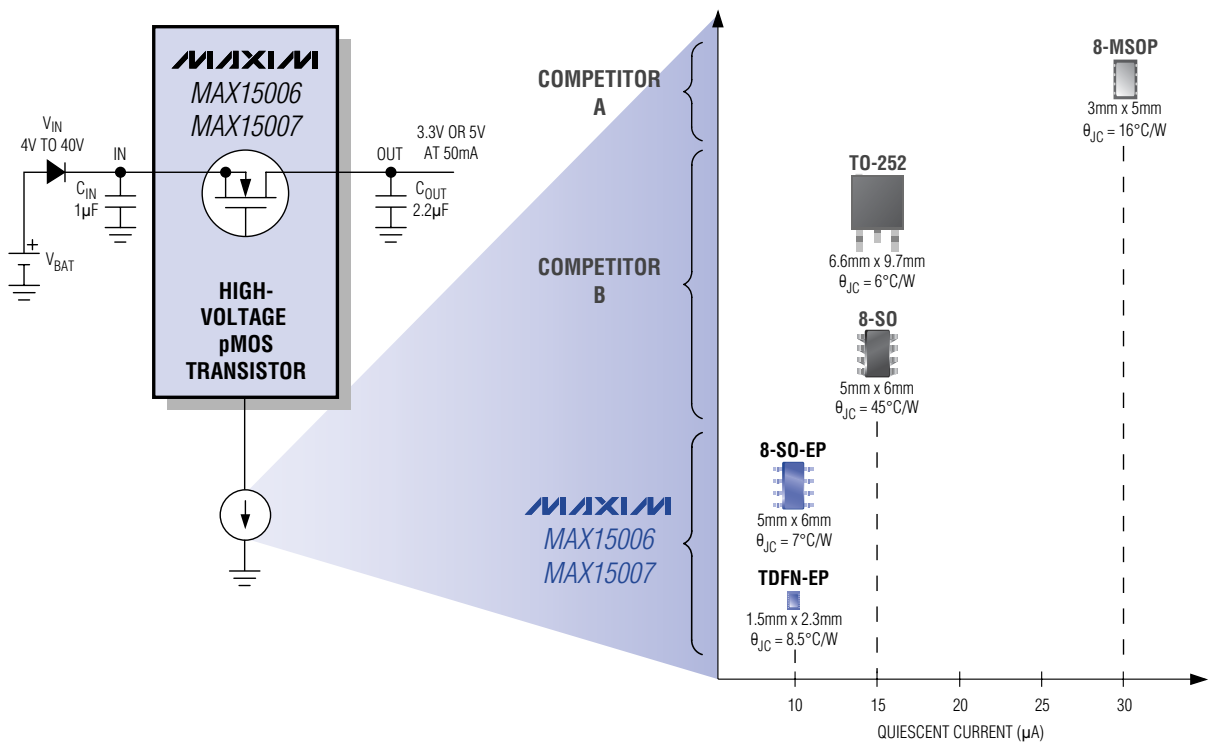
16-Pin TQFN Package Is 60% Smaller than Competitor's DPAK



50mA, 10µA I_Q, Automotive LDO Regulators Are Best Choice for Always-On Applications

The MAX15006/MAX15007 internal high-voltage, p-channel MOS pass transistors provide low 10µA quiescent current and low-dropout operation from 4V cold-crank to 40V load dump.

IDEAL FOR TPMS, RKE, CAR ALARM, AND OTHER ALWAYS-ON APPLICATIONS



- **Wide Operating Input-Voltage Range (4V to 40V)**
- **Guaranteed 50mA Output Current**
- **Low Quiescent Current 10µA (No Load) and 90µA (Full Load)**
- **Operates Through Cold-Crank Condition**
- **Withstands 45V Load Dump**
- **300mV Low Dropout Voltage (MAX15006B/MAX15007B)**
- **Stable Operation with Tiny 2.2µF Output Capacitor**
- **Enable Input (MAX15007)**
- **Preset 3.3V and 5.0V Output Voltages**
- **Thermal and Short-Circuit Protection**

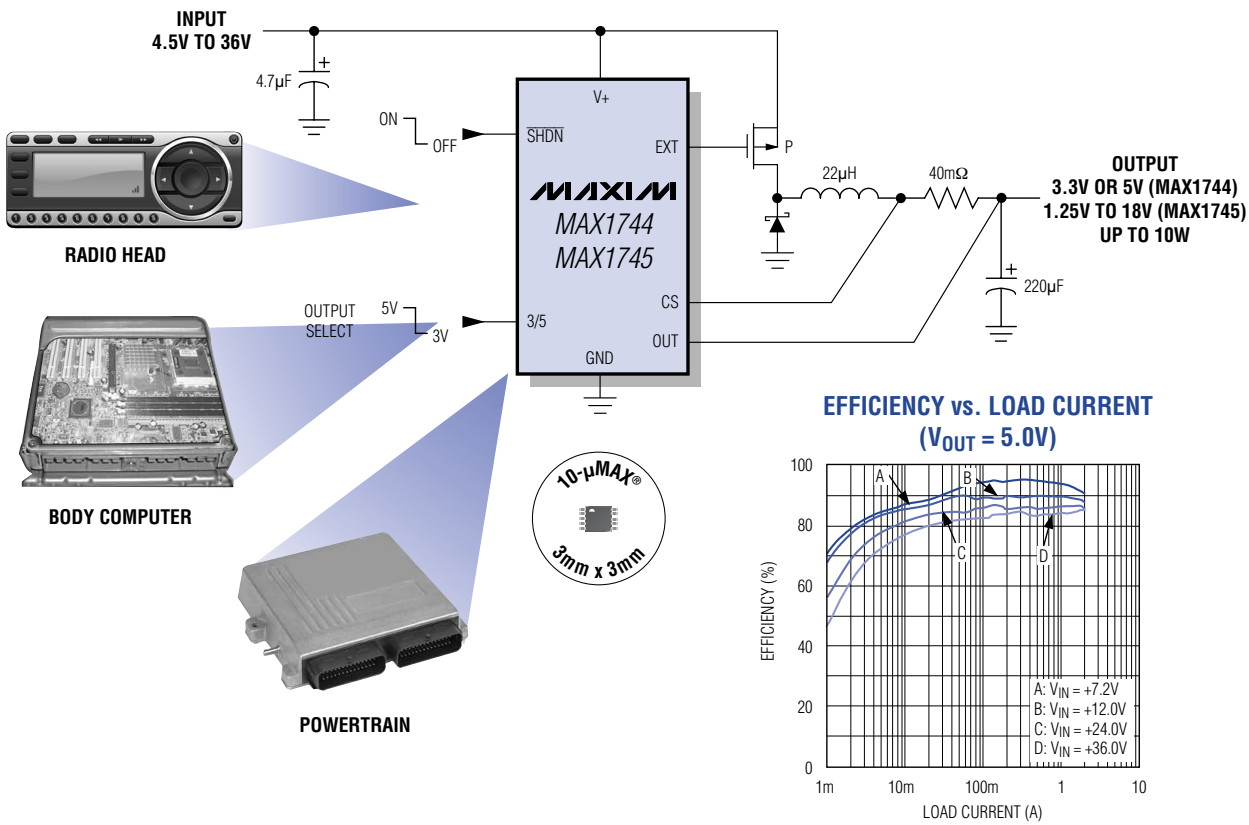
Low I_Q Automotive Linear Regulators

Part	I_Q (µA)	Input Voltage (V)	Output Voltage (V)	Output Current (mA)	Package (mm x mm)
MAX15006	10 (no load), 90 (full load)	4 to 40	3.3 or 5	50	6-TDFN (3 x 3), 8-SO
MAX15007	10 (no load), 90 (full load)	4 to 40	3.3 or 5	50	6-TDFN (3 x 3), 8-SO
MAX5086	70 (no load), 13 (shutdown)	6.5 to 65	3.3 or 5 (preset), 2.5 to 11 (adj)	250	16-/56-TQFN
MAX5087	70 (no load), 11 (shutdown)	6.5 to 65	3.3 or 5 (preset), 2.5 to 11 (adj)	400	16-/56-TQFN
MAX5023/MAX5024	60 (no load)	6.5 to 65	3.3 or 5, 11 (adj, MAX5024)	150	8-SO-EP
MAX5084/MAX5085	50	6.5 to 65	3.3 or 5 (preset), 2.54 to 11 (adj)	200	6-TQFN (3 x 3)

Small 36V Input, 10W Output Step-Downs Have Low 90µA Supply Current

Simple Controllers Fit in µMAX Package and Are 95% Efficient

The MAX1744/MAX1745 are small, simple, high-efficiency step-down controllers. Their wide input range, low supply current, high output power, and high efficiency make them popular in automotive applications. External component size is minimized by their high 330kHz switching frequency and their proprietary current-limited control scheme. They also feature 100% duty-cycle operation for low-dropout operation.



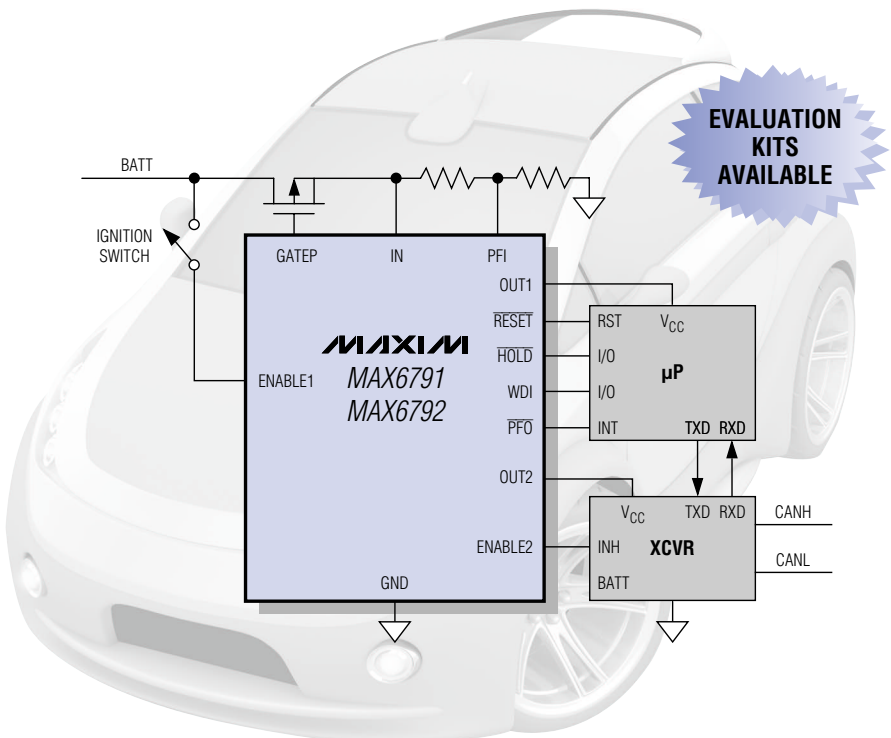
- 4.5V to 36V Input
- Drives Low-Cost p-Channel Switch
- Only 90µA Quiescent Supply Current
- Up to 95% Efficiency
- 1.25V to 18V Output (MAX1745)
- Fixed 3.3V or 5V Output (MAX1744)
- Small, 10-Pin µMAX Package
- EV Kit Available to Speed Designs

For More Information About *Choosing the Right DC-DC Converter for Automotive Applications*, Go to: www.maxim-ic.com/AN1845

µMAX is a registered trademark of Maxim Integrated Products, Inc.

72V Input, 300mA, Single-/Dual-Output Linear Regulators Are Ideal for Automotive Applications

Integrate Supervisory Functions and Consume Only 68µA Supply Current



High Performance

- Operate from 5V to 72V
- 68µA Low-Quiescent Current
- Thermal, Short-Circuit, and Load-Dump Protection

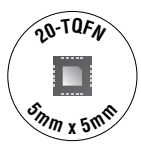
Flexibility

- Open-Drain/Push-Pull Outputs
- Fixed or Capacitor-Adjustable Reset and Watchdog Timeouts

High Integration

- Single/Dual Outputs
- Window (min/max) Watchdog
- Reset/Power-Fail Comparator
- Enable and Hold Circuit
- Reverse-Battery Protection

Part	V_{IN} Range (V)	Junction Temperature Range (°C)	I_{OUT} (mA)	Output Configuration	Output Voltage (V)
MAX6791–MAX6794	5 to 72	-40 to +150	150	Dual	Fixed 5, 3.3, 2.5, 1.8, or 1.8 to 11 (adj)
MAX6795/MAX6796			300	Single	

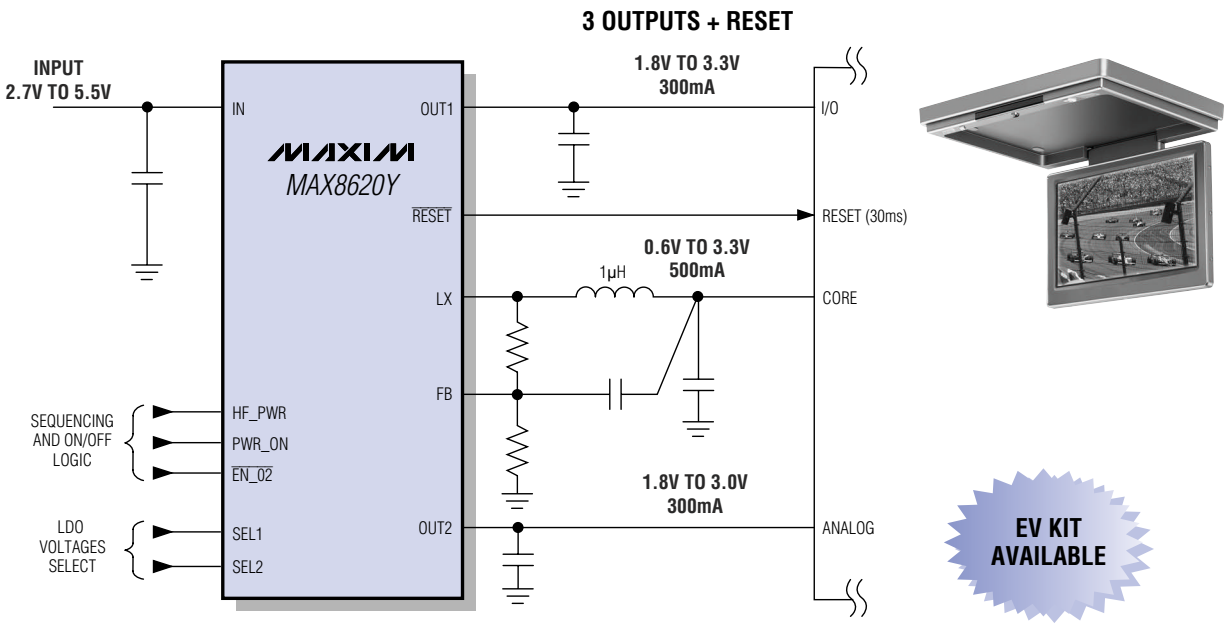


THERMALLY ENHANCED PACKAGE

DALLAS SEMICONDUCTOR MAXIM

PMIC in a 3mm x 3mm TDFN Integrates Two LDOs Plus Reset

500mA Output and over 90% Efficiency for µP-Based Rear-Seat Entertainment

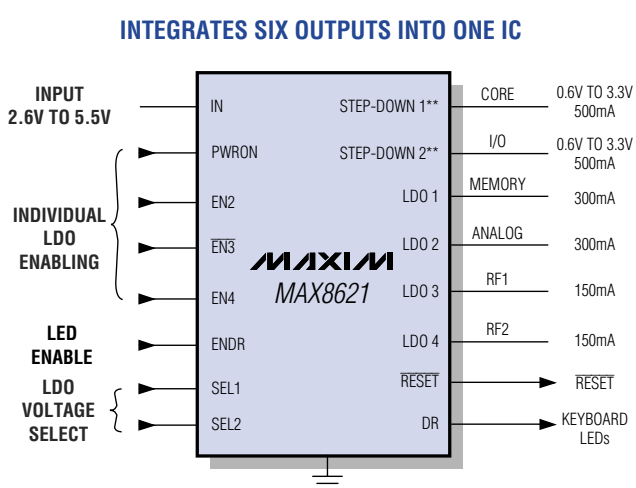


- 500mA, Step-Down DC-DC Output Down to 0.6V
- Internal Synchronous Rectifier Provides Up to 92% Efficiency
- Internal Soft-Start Eliminates Inrush Current
- Two 45µV_{RMS} Low-Noise LDOs
- Pin-Selectable LDO Regulators

Smallest 6-Output PMIC Has 92% Efficiency

Highly Configurable for Your POL* Automotive Application

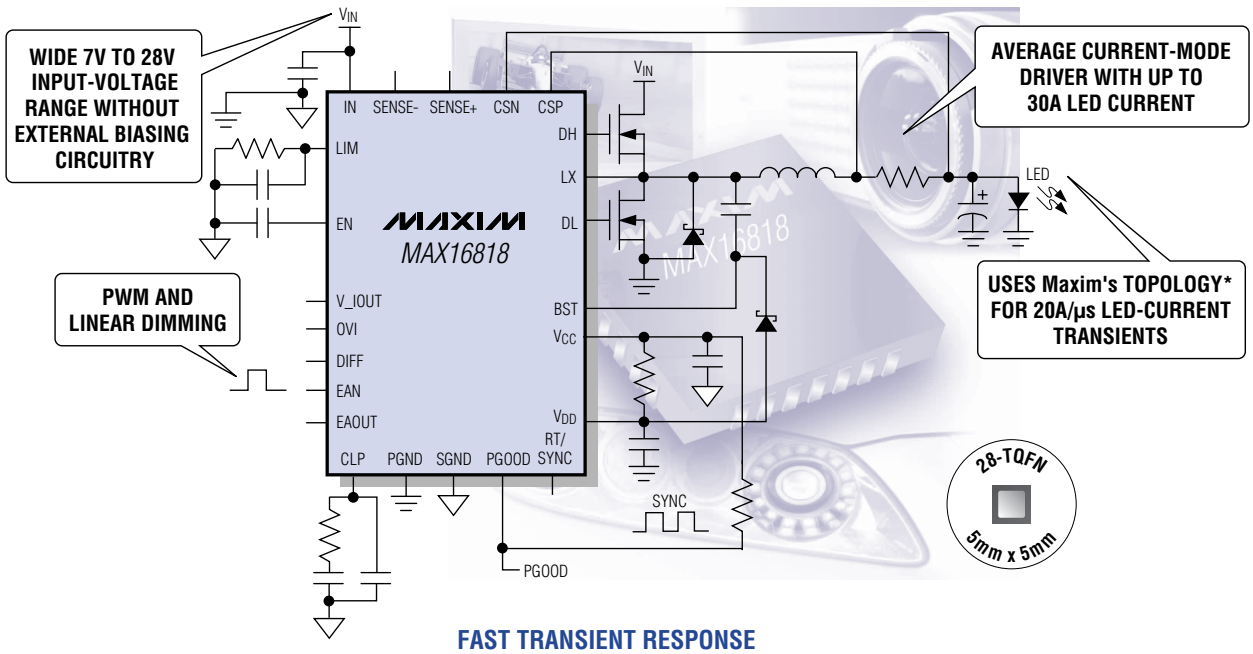
- Small, 4mm x 4mm, 24-Pin TQFN
- 4MHz Step-Down DC-DC Uses 1µH Inductor
- Internal Synchronous Rectifier for Up to 92% Efficiency
- 45µV_{RMS} Low-Noise LDOs
- Pin-Selectable LDO Output Voltages
- Internal Soft-Start for No Inrush Current



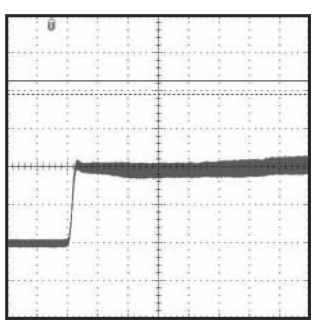
*Point-Of-Load
**Needs external components

First High-Power LED Driver with Rapid Transient Response

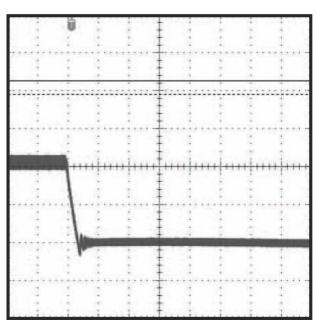
MAX16818 Has Over 91% Efficiency



FAST TRANSIENT RESPONSE



M 1.00µs
0 TO 10A: t_{RISE} < 500ns



M 1.00µs
10A TO 0: t_{FALL} < 500ns

Features

- Suitable for Buck, Boost, Buck-Boost, SEPIC, and Cuk Topologies
- 125kHz to 1.5MHz Programmable Switching Frequency
- Wide -40°C to +125°C Temperature Range
- Overvoltage Protection, Thermal Shutdown

Applications

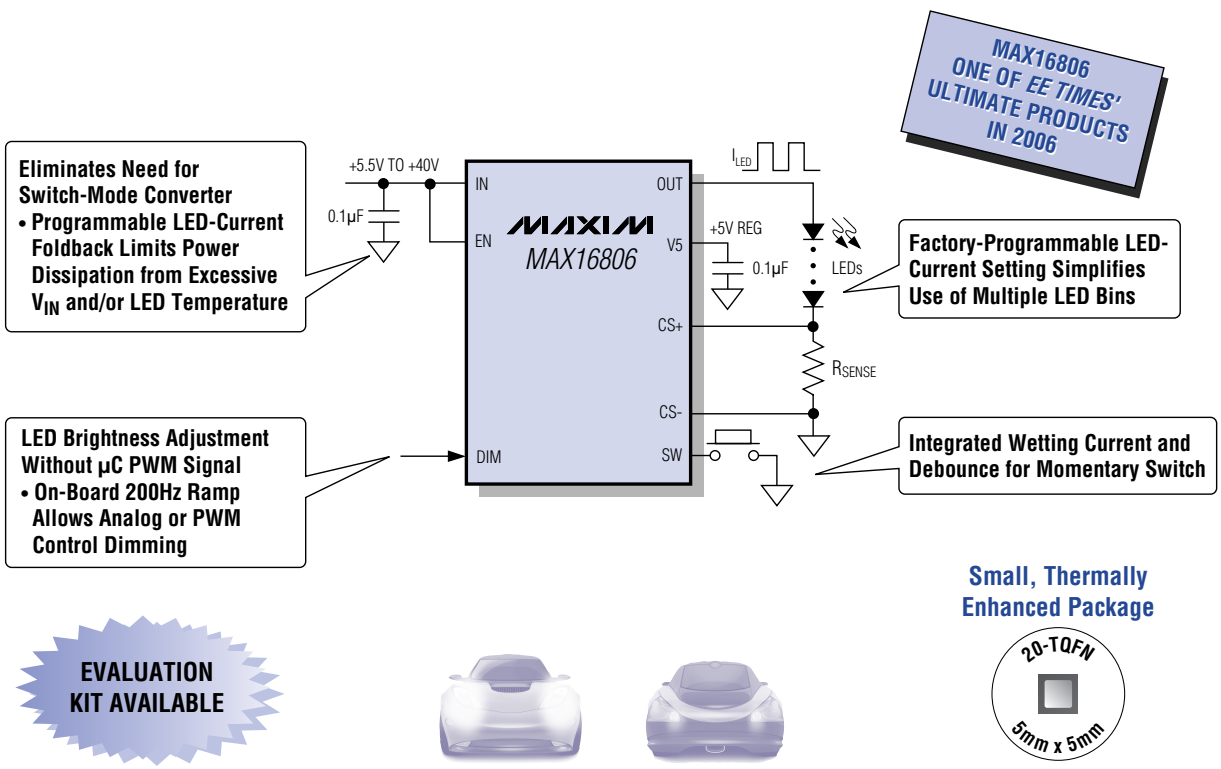
- RSE LCD and Display Backlighting
- Automotive and Bus/Truck Exterior Lighting
- Automotive Emergency Lighting and Signage

For More LED Solutions, Go to: www.maxim-ic.com/LED

*Patent pending.

First High-Current Linear LED Driver Eliminates the Need for µC and Switch-Mode Converter

Ideal for Automotive Lighting Applications; Reduces Cost and EMI



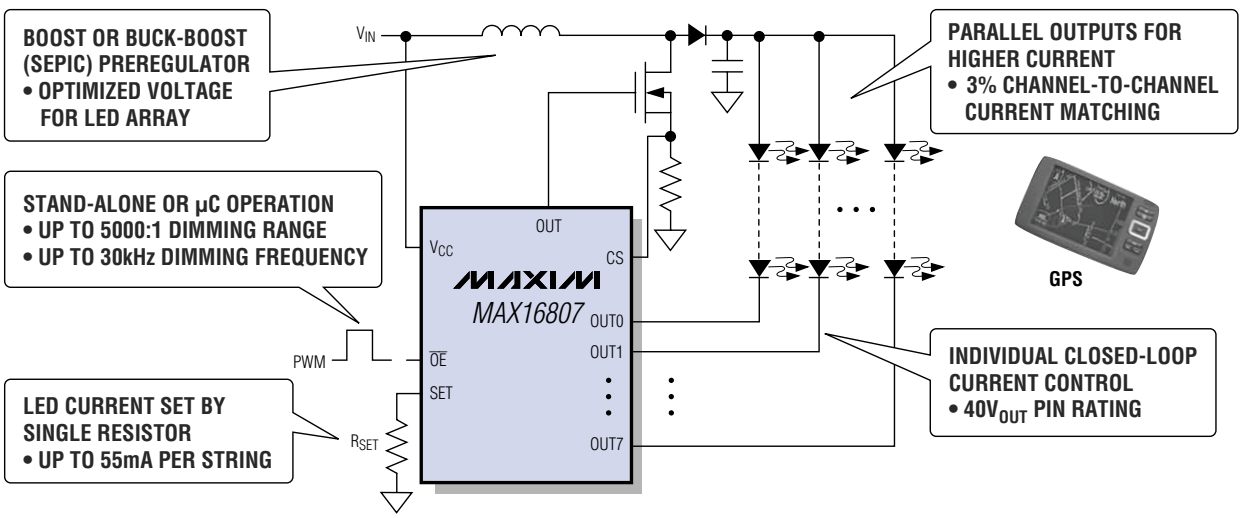
350mA LED Driver Family

Part	EN Pin	3.5% LED-Current Accuracy	Load-Dump Protected (45V)	5V Output	DIM Input	DIM with DC Signal	V_{IN} Programmable LED-Current Foldback	Programmable LED-Current Reference	Programmable Thermal Foldback	Momentary-Switch Interface
MAX16800	✓	✓	✓	✓	✓					
MAX16803										
MAX16804						✓				
MAX16805						✓	✓	✓		
MAX16806						✓	✓	✓	✓	✓

Highest Integration LED Drivers for White- and RGB-LCD Backlighting

High-Efficiency PWM Controller Has 8 or 16 Constant-Current Channels

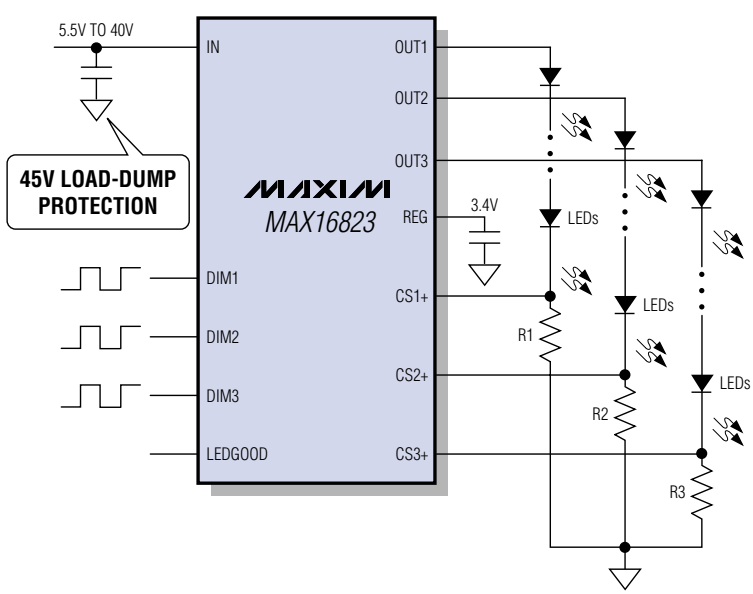
IDEAL FOR AUTOMOTIVE NAVIGATION, HEADS-UP, AND INFOTAINMENT DISPLAYS



Part	Open-LED Detection	No. of Channels	Package (mm x mm)
MAX16807/MAX16808*	— / ✓	8	28-TSSOP-EP (6.4 x 9.7)
MAX16809/MAX16810*	— / ✓	16	38-TQFN (5 x 7)

Highest Integration, 3-Channel Linear LED Driver Has Open-LED Detection

- Adjustable Constant LED Current (Up to 70mA, 2A with External BJT)
- ±5% LED Current Accuracy
- Low Dropout Voltage (0.7V, max)
- +3.4V Regulator with 4mA Capability
- Undervoltage Lockout
- Short-Circuit Protection
- Thermal Shutdown
- Ideal for Automotive Lighting (RCL, CHMSL, RGB Ambient)



*Future product—contact factory for availability.

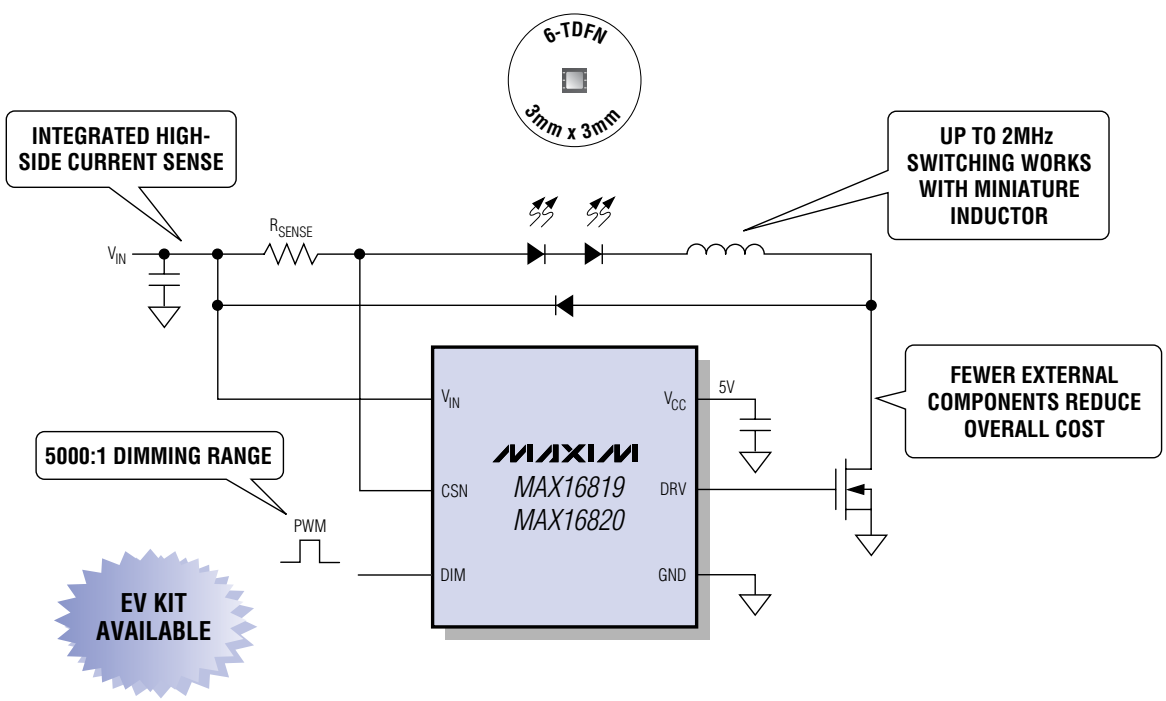
DALLAS SEMICONDUCTOR MAXIM

Smallest, High-Efficiency, High-Brightness LED Drivers Save Space and Cost

Ideal for Automotive Exterior/Interior Lighting

The MAX16819/MAX16820 step-down, constant-current high-brightness LED (HB LED) drivers provide a cost-effective design solution for automotive interior/exterior lighting. These devices operate from a 4.5V to 28V input-voltage range and provide up to 0.5A of source and 1A of sink drive capability to an external MOSFET. A high-side current-sense resistor adjusts the output current, and a dedicated PWM input (DIM) enables a wide range of pulsed dimming.

The MAX16819/MAX16820 are well suited for applications requiring a wide input-voltage range. The high-side current sensing and integrated current-setting circuitry minimize the number of external components while delivering an LED current with ±5% accuracy. A hysteretic control algorithm ensures excellent input-supply rejection and fast response during load transients and PWM dimming. The MAX16819 features a 30% current ripple, and the MAX16820 has a 10% current ripple. These devices operate up to a 2MHz switching frequency, thus allowing small component size.



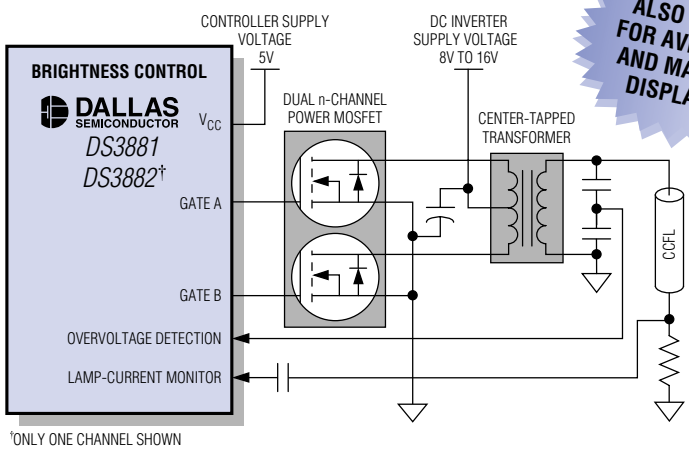
- 4.5V to 28V Input-Voltage Range
- ±5% LED Current Accuracy
- 0.5A Source/1A Sink Gate Drive
- 5V Regulator with 4mA Capability
- Operate from -40°C to +125°C

Download a Design Calculator for the MAX16819/MAX16820 at:
www.maxim-ic.com/MAX16819-20-Tool

Automotive CCFL Controllers Reduce EMI and Provide 300:1 Dimming

Lowest Component Count, Feature-Rich, Automotive Inverter Solutions for LCDs and Control-Panel Backlighting

LAMP-CURRENT OVERDRIVE MODE FOR QUICK STARTUP IN COLD CONDITIONS



†ONLY ONE CHANNEL SHOWN

ALSO IDEAL FOR AVIATION AND MARINE DISPLAYS

EMI-Reduction Features

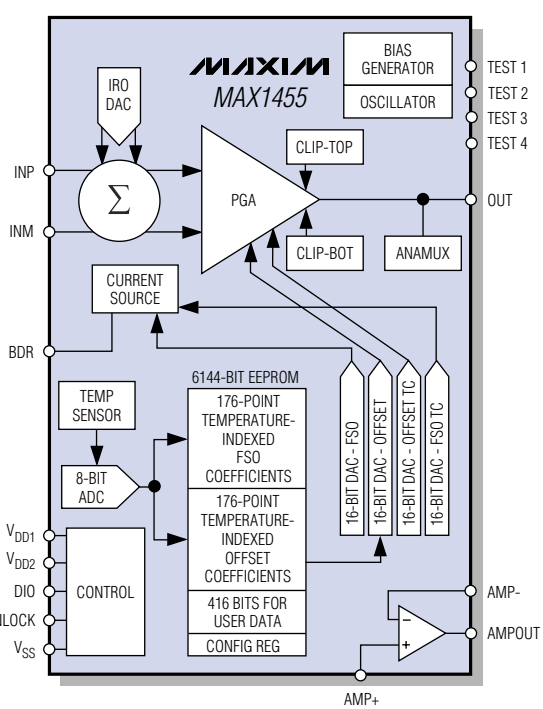
- Optional Spread-Spectrum Function for Lamp Clock
- Dynamically Step Lamp Frequency Up or Down to Move EMI Spurs from Radio Band

Highly Integrated Solution

- High-Density CCFL Controllers for One- and Two-Lamp Automotive LCDs and Control-Panel Backlighting
- Wide -40°C to +105°C Temperature Range

Diagnostic Output for Automotive ECUs

- Single-Pin Digital Programming
- Fully Analog Signal Path
- Accommodates Sensor Output Sensitivities from 5mV/V to 40mV/V
- 16-Bit Offset and Span Calibration Resolution
- On-Chip Lookup Table Supports Multipoint Calibration Temperature Correction
- Selectable-Output Clipping Limits



DALLAS SEMICONDUCTOR MAXIM

Low-EMI, High-ESD-Protection, and Low-I_Q Audio Solutions

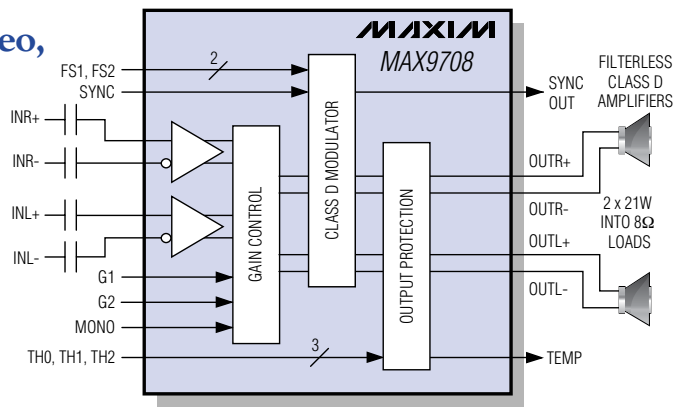
Ideal for Infotainment Applications

FOR Maxim's COMPLETE LINE OF AUDIO SOLUTIONS, GO TO: www.maxim-ic.com/audio

Low EMI

Filterless, Spread-Spectrum, Mono/Stereo, Class D Amplifier (MAX9708)

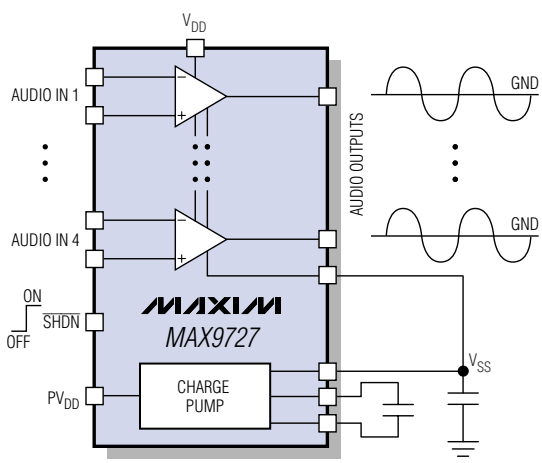
- Unique Patented* Spread-Spectrum Mode Reduces EMI
- High Efficiency Up to 87%
- High PSRR (90dB at 1kHz)
- Differential Inputs
- Shutdown and Mute Control
- Integrated Click-and-Pop Suppression



High ESD Protection

Quad Audio Line Driver with 3V_{RMS} Output (MAX9727)

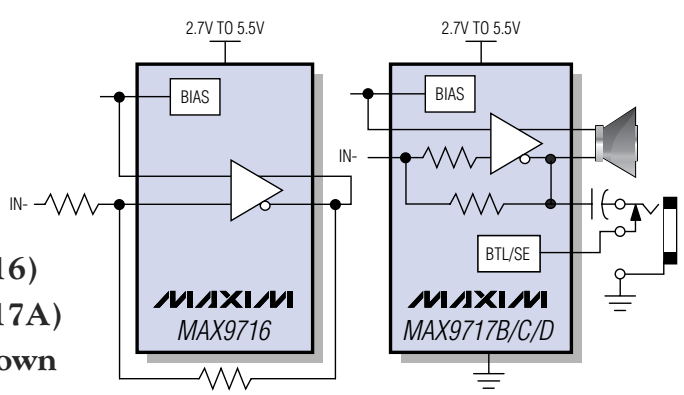
- ±8kV HBM ESD-Protected Outputs
- High 100dB PSRR
- 109dB Signal-to-Noise Ratio
- No Audible Clicks or Pops at Power-Up/Down
- Differential Inputs
- 2.7V to 5.5V Single-Supply Operation



Low I_Q

Mono, 1.4W BTL Audio Power Amplifiers (MAX9716/MAX9717)

- 10nA Low-Power Shutdown Mode
- 73dB PSRR at 1kHz
- 2.7V to 5.5V Single-Supply Operation
- Pin Compatible with LM4890 (MAX9716)
- Pin Compatible with TPA711 (MAX9717A)
- No Audible Clicks/Pops at Power-Up/Down



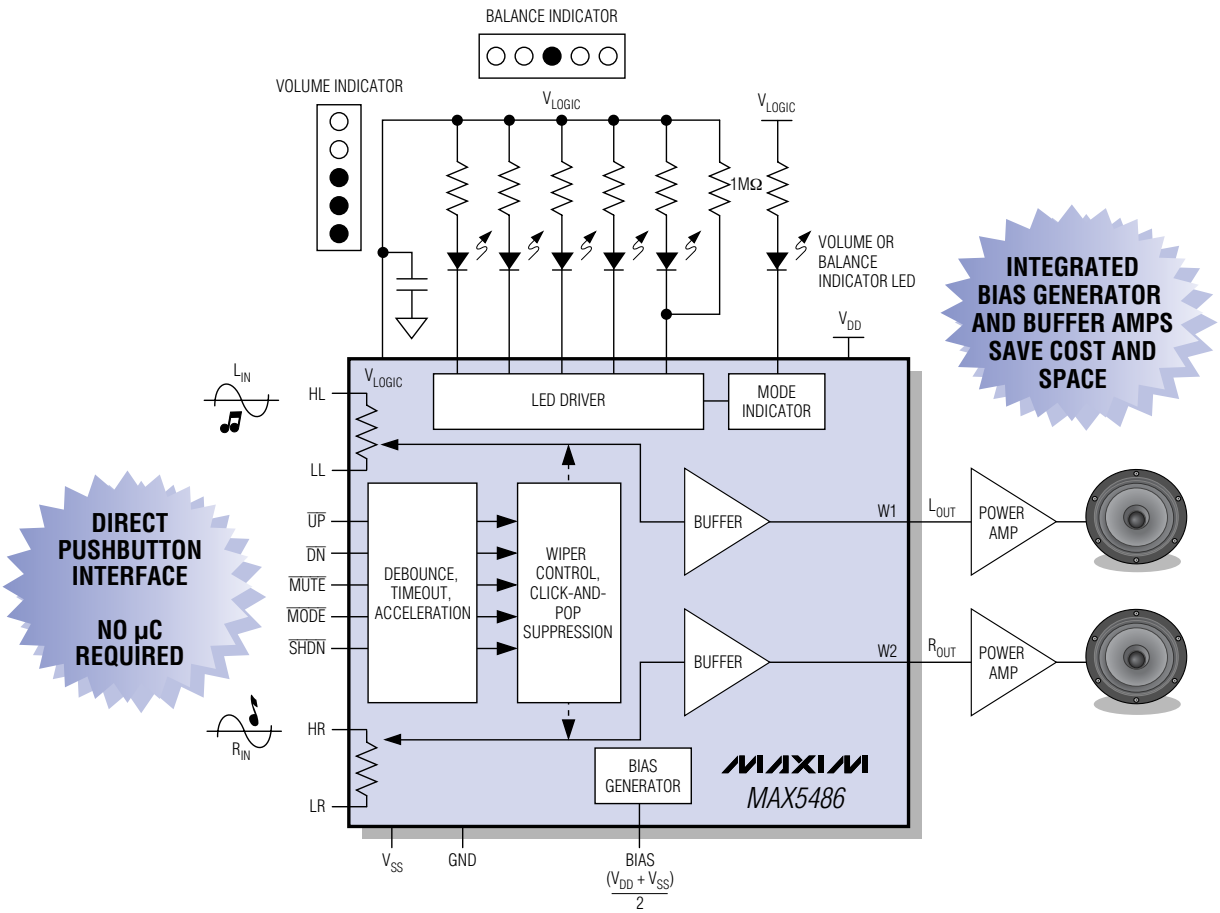
*U.S. Patent #6,847,257

NEW

Pushbutton Stereo Volume and Balance Controller Has 5-Segment LED Driver

Integration Saves Space, No µC Needed

The MAX5486 volume and balance controller features Maxim's proprietary enhanced SmartWiper™ architecture. SmartWiper eliminates the need for a µC by automatically advancing the wiper at a rate of 4Hz for presses between 250ms and 500ms, at a rate of 8Hz for presses between 500ms and 1s, and at a rate of 11Hz for presses > 1s.

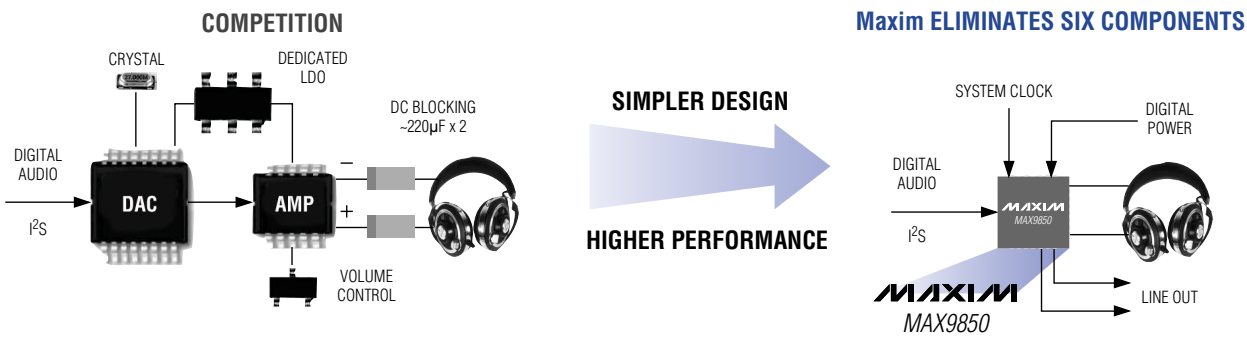


- **Debounced Pushbutton Interface Directly Controls Volume and Balance**
- **Integrated Low-Power Wiper Buffers Provide 0.003% THD+N**
- **SmartWiper Control with Accelerated Autoadvance**
- **Clickless Switching**
- **Integrated Bias Generator**
- **5-Segment LED-Indicator Driver Provides Volume or Balance Level**
- **32-Tap Log Taper with 2dB Step Size**
- **Power-On Reset to -12dBFS Wiper Position**
- **-90dB Mute**

SmartWiper is a trademark of Maxim Integrated Products, Inc.

18-Bit Stereo Audio DAC Eliminates Large, Costly Components and Produces 30mW from 1.8V

-100dB PSRR and Built-In DirectDrive™ Headphone Amplifiers Eliminate LDO and Two DC-Blocking Capacitors

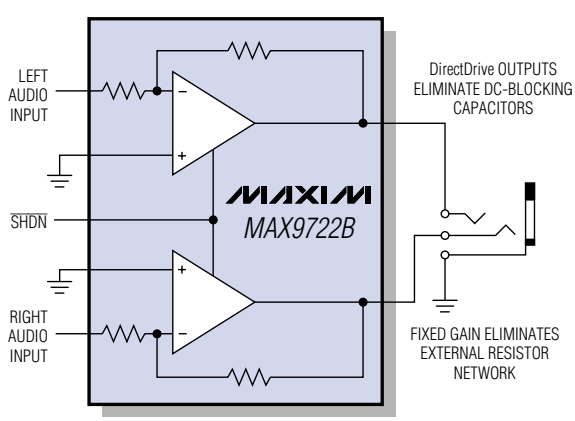


- DirectDrive Outputs Eliminate DC-Blocking Caps Without Biasing the Chassis
- Derives Common Audio Sample Rates from Existing System Clocks Up to 40MHz, thus Eliminating External Crystals
- Integrated Digital Headphone Volume and Mute Control
- Stereo Line Inputs and Outputs ($2V_{RMS}$)
- 1.8V to 3.6V Single-Supply Operation

28-QFN 5mm x 5mm x 0.8mm

High-ESD-Protection, DirectDrive, 130mW Stereo Headphone Amp with Shutdown

- ±8kV ESD Protection
- High PSRR (80dB at 217Hz) Eliminates LDO
- No Bulky DC-Blocking Capacitors Required
- Differential Inputs
- Low 0.009% THD+N
- Integrated Click-and-Pop Suppression
- 2.4V to 5.5V Single-Supply Operation

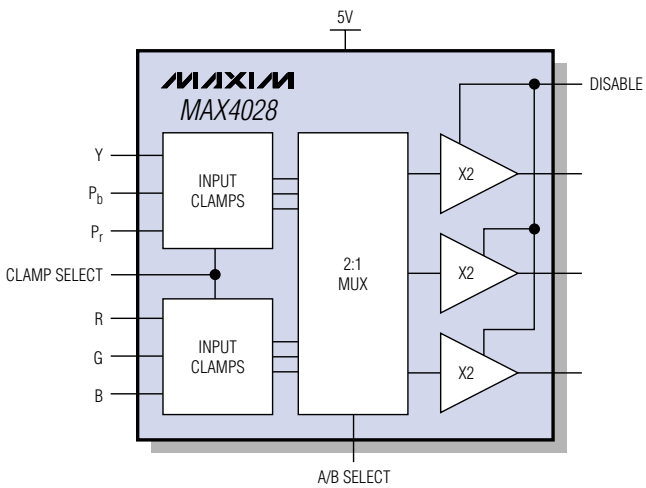


Triple/Quad 2:1 Mux-Amps for Component and VGA Signals

Selectable Sync-Tip and Keyed Clamps Simplify Input-Source Selection and Eliminate Up to 48 Discrete Components

- Selectable Input Sync-Tip and Keyed Clamps Are Ideal for Video-Source Switching
- Directly Drives 150Ω Back-Terminated Video Loads
- Variable Keyed-Clamp Reference Voltage
- Output Disable Supports Multiple Devices for Larger Systems
- 20ns Channel Switching and Low ±10mV$_{P-P}$ Transients Suitable for On-Screen Display (OSD) Insertion

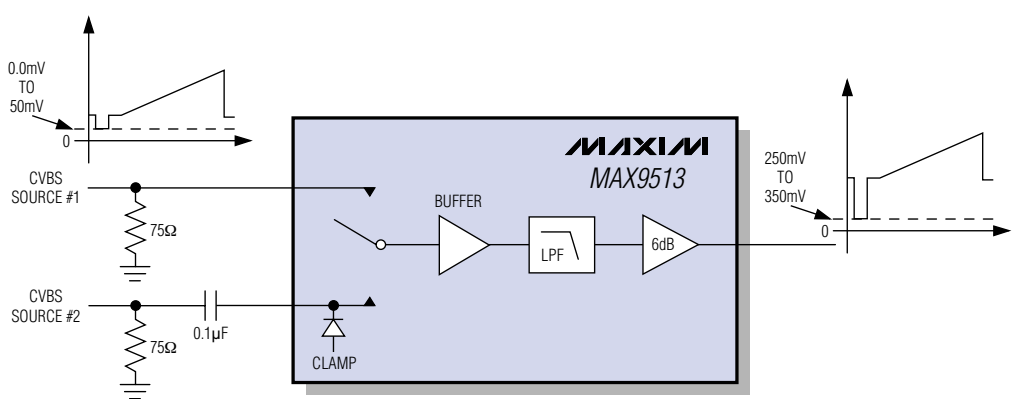
IDEAL FOR AUTOMOTIVE NAVIGATION/INFOTAINMENT



2:1 Mux-Amps for Your Video Infotainment Applications

Bidirectional Composite Video Signal, Single-Supply Operation, and Two Composite Inputs/Outputs

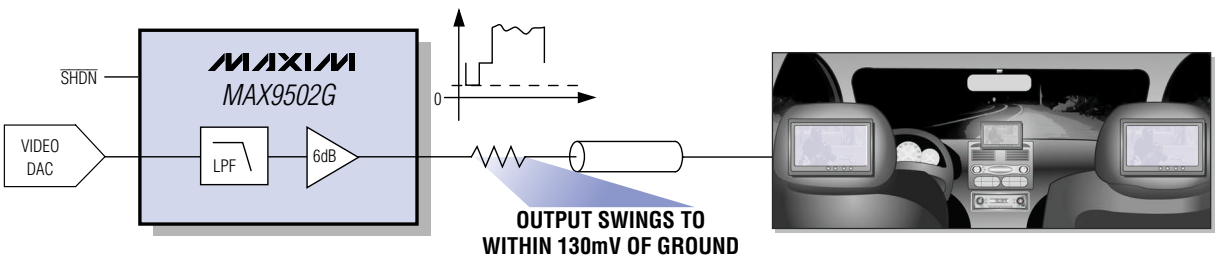
The MAX9513 CVBS video filter amplifier with SmartSleep and bidirectional video support is ideal for rear-seat entertainment centers. The input can be directly connected to the DAC output.



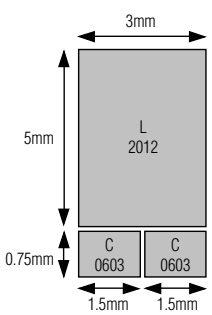
- 3.3V Operation
- SD Video Reconstruction Filters
- Sync-Tip Clamp on One Input Channel
- AC- or DC-Coupled Outputs
- Available in a 3mm x 3mm, 16-Pin TQFN Package

Industry's Smallest Video-Filter Amplifier Is Ideal for Rear-Seat Entertainment

Up to 12x Smaller and Consumes Up to 1.5x Less Power than the Competition



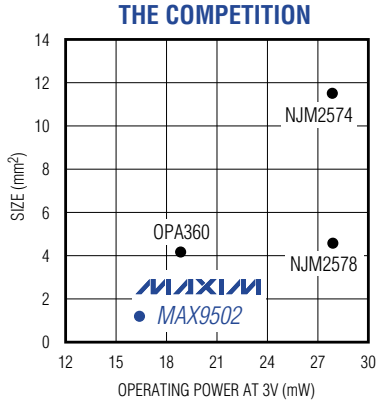
TYPICAL SOLUTION (L-C π FILTER)



VS.

Maxim's µDFN SOLUTION IS 12x SMALLER

SIZE vs. POWER—MAX9502 OUTPERFORMS THE COMPETITION



Saves Space

- Tiny 1mm x 1.5mm µDFN Package Is Up to 12x Smaller than the Competition
- Output Swings to Within 130mV of Ground—Eliminates Bulky Output Caps
- Integrated Video Reconstruction Filter
- DC Couples Directly to Video DAC Outputs—No Input Cap Needed

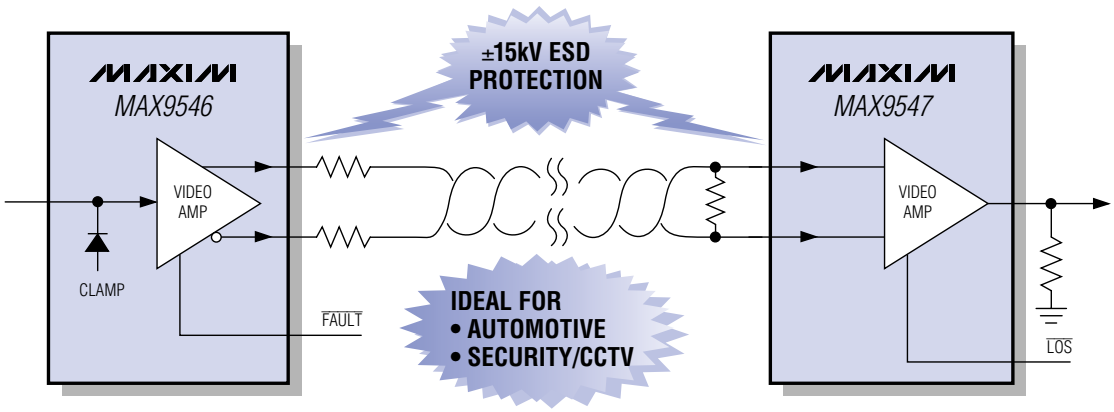
Saves Power

- 10nA Shutdown Current—Up to 500x Less than the Competition
- Low 2.5V to 3.6V Operation
- 5.3mA Quiescent Supply Current—12% Less Power Consumption than Nearest Competitor

Part	Input Coupling	Output Coupling	Gain (dB)	Supply Voltage (V)	Shutdown Current (nA)	Package
MAX9502G	DC	DC	6	2.5 to 3.6	10	6-µDFN/5-SC70
MAX9502M			12			

Industry's First Differential Video Driver/ Receiver Chipset with Diagnostic Capability

Fault and LOS-Detection Circuitry Instantly Identifies and Reports Failures; Robust Input/Output Survives Shorts to Ground and Battery



Intelligent Diagnostics

- Fault and Short Detection (MAX9546)
- Loss-of-Signal Detection (MAX9547)

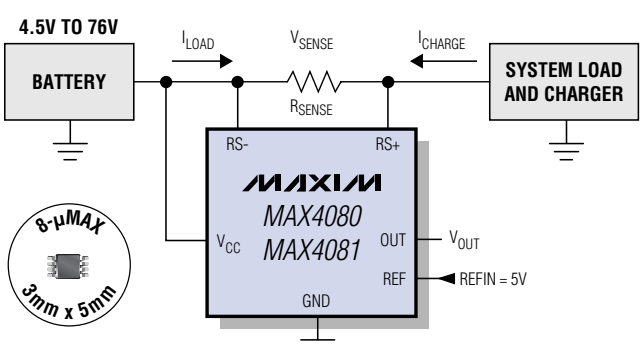
Convenience and Low Total-Solution Cost

- Transmit Signals in Readily Available, Lower Cost, Unshielded Twisted Pairs vs. Coax Cable

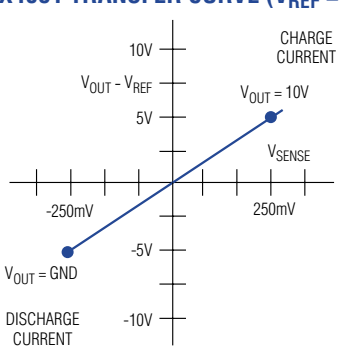
Robust Performance

- Provide ±15kV ESD Protection (Human Body Model)
- Withstand ±2V Ground-Level Shift Between Source and Load
- Survive Shorts to Ground or High-Battery Conditions (16V)
- Reduce EMI; Less Susceptible to Noise

Dedicated Current-Sense Amplifiers for Current Monitoring and Control



MAX4081 TRANSFER CURVE (V_{REF} = 5V)

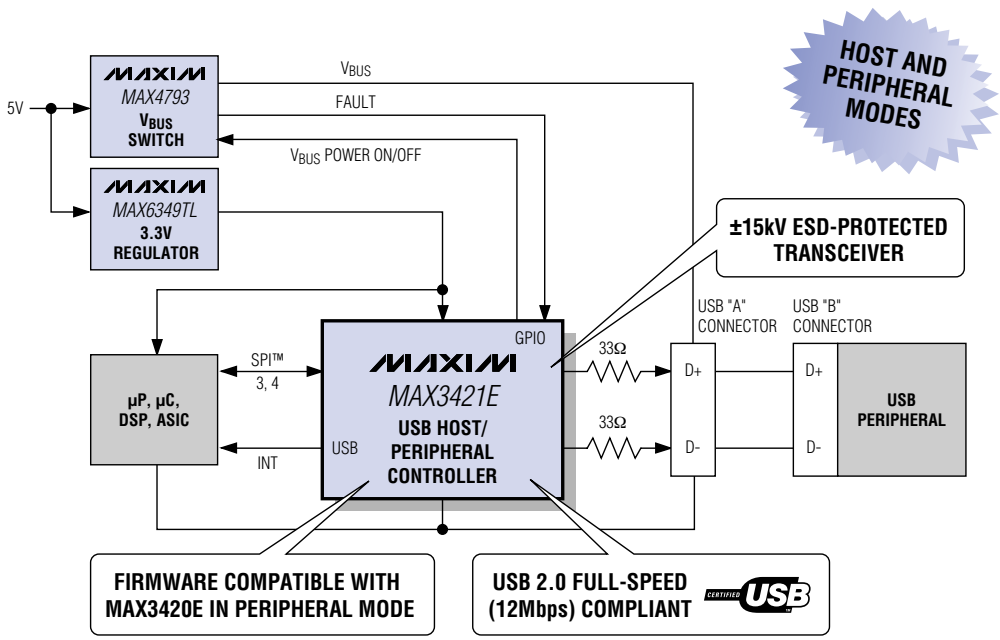


Ideal for

- 12V, 24V, or 42V Automotive Batteries
- Bidirectional (MAX4081) and Unidirectional (MAX4080) Motor Control
- Power-Management Systems
- Precision High-Voltage Current Sources

Add USB Host Functionality with a Single IC

Make Your µP, µC, DSP, or ASIC a Full-Speed USB Host/Peripheral for Your Infotainment Application



MAX3421 Features

- ±15kV ESD-Protected, Integrated Full-Speed USB Transceiver (12Mbps)
- SPI Interface to the Register Set (Up to 26MHz)
- Extra I/Os: 8 General-Purpose Inputs and 8 General-Purpose Outputs
- 5mm x 5mm, 32-Pin TQFN Package

Host-Mode Features

- Automatically Generates Start Frames
- 256 Bytes of FIFO for USB Data Transfers
- Supports Control, Bulk, Interrupt, and Isochronous Transfers
- Ideal for MP3 Players and PDA Cell Phones

Peripheral-Mode Features

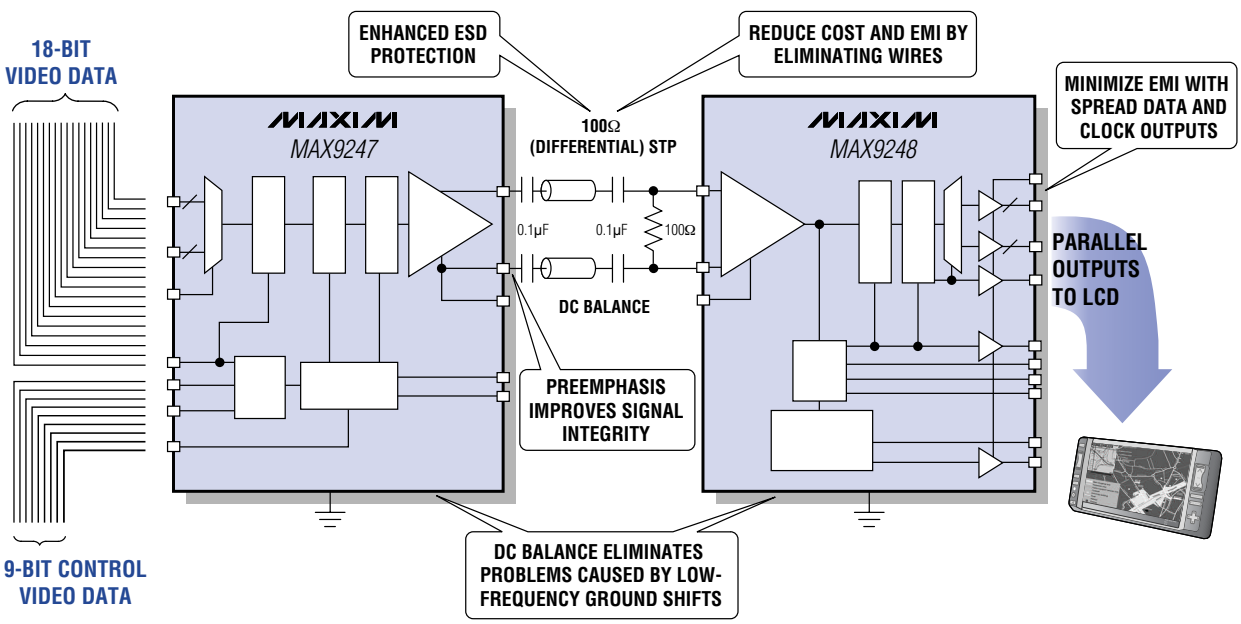
- Supports Four Endpoints
- 392 Bytes of FIFO for USB Data Transfers
- Supports Control, Bulk, and Interrupt Transfers

SPI is a trademark of Motorola, Inc.

27-Bit LVDS Serializers/Deserializers for Automotive Navigation Systems

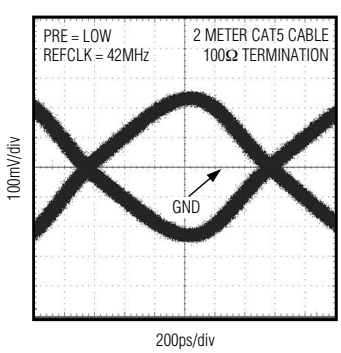
Programmable Spread Spectrum, Feeds Up to 1280 x 480 Displays

The MAX9247/MAX9248/MAX9250 27-bit, DC-balanced serializers/deserializers (SerDes) feature preemphasis and programmable spread-spectrum capability, which spreads both output data and clock for maximum EMI reduction. The spread is programmable for ±4%, ±2%, or no-spread (MAX9250). Preemphasis improves signal integrity at the load over 10m cables. The MAX9247/MAX9248/MAX9250 are ideal for driving WVGA, VGA, and QVGA displays.

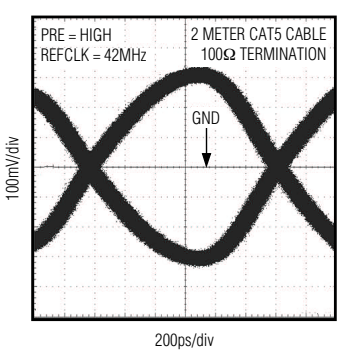


PREEMPHASIS IMPROVES EYE DIAGRAM

EYE DIAGRAM WITHOUT PREEMPHASIS

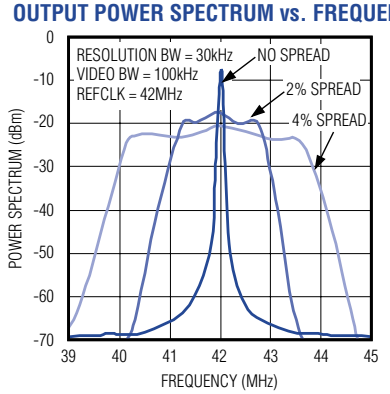


EYE DIAGRAM WITH PREEMPHASIS



SPREAD SPECTRUM REDUCES EMI

OUTPUT POWER SPECTRUM vs. FREQUENCY



Serializers

Part	Clock (MHz)	Features
MAX9247	2.5 to 42	Output common-mode filter, selectable preemphasis
MAX9217	3 to 35	Output common-mode filter

Deserializers

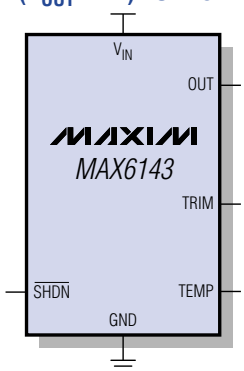
Part	Clock (MHz)	Features
MAX9248	2.5 to 42	Selectable ±2% or ±4% spread spectrum
MAX9250	2.5 to 42	Output enable
MAX9218	3 to 35	Output enable

High-Performance, High-Precision Voltage References Are Guaranteed over the Automotive Temperature Range

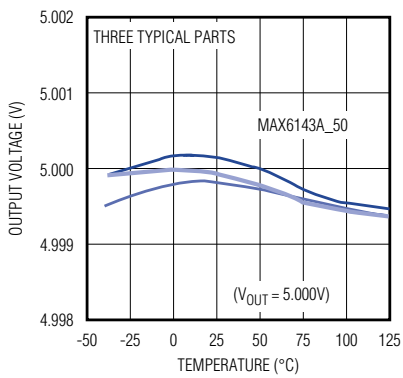
Wide Input Range and Low Output-Voltage Temperature Drift

Part	Output Voltage (V)
MAX6037_12	1.25
MAX6037_21	2.048
MAX6037_25	2.5
MAX6033_30	3.0
MAX6037_33	3.3
MAX6033_41	4.096
MAX6033_50	5.0
MAX6143_50	5.0
MAX6043_10	10.0

INPUT RANGE FROM (V_{OUT} + 2V) TO +40V



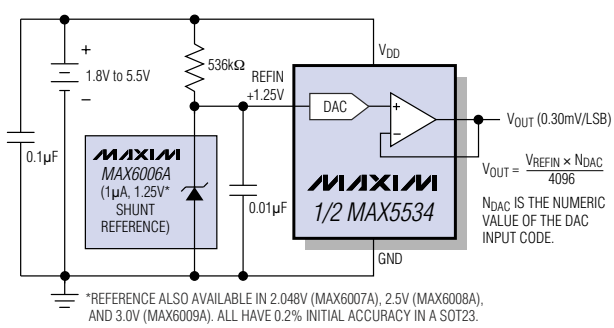
LOW TEMPERATURE COEFFICIENT



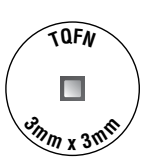
Large Selection of Precision DACs that Save Space

Ultra-Small 3mm x 3mm DACs Simplify Designs

- Low Power (Down to 1.8V at 5µA)
- Serial Interfaces Compatible with SPI or I²C Protocols
- 2.7V to 5.5V Single-Supply Voltage Range
- Buffered Voltage Outputs Swing Rail-to-Rail
- Micropower Shutdown Mode to 1µA (max)
- 6-Bit to 24-Bit Resolution



*REFERENCE ALSO AVAILABLE IN 2.048V (MAX6007A), 2.5V (MAX6008A), AND 3.0V (MAX6009A). ALL HAVE 0.2% INITIAL ACCURACY IN A SOT23.



27 Automotive DACs in 3mm x 3mm

Package	No. of DACs Available
5-SOT23	6
6-SOT23	10
8-SOT23	2
8-TQFN	1
12-TQFN	6
16-TQFN	2

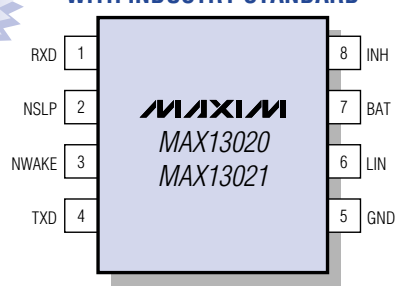
Industry's Best Overall LIN Bus Transceivers

10x Lower LIN Bus Short-to-Ground Current, Wider Overvoltage-Protection Range (±60V), 3x ESD Protection, Lowest Shutdown Current

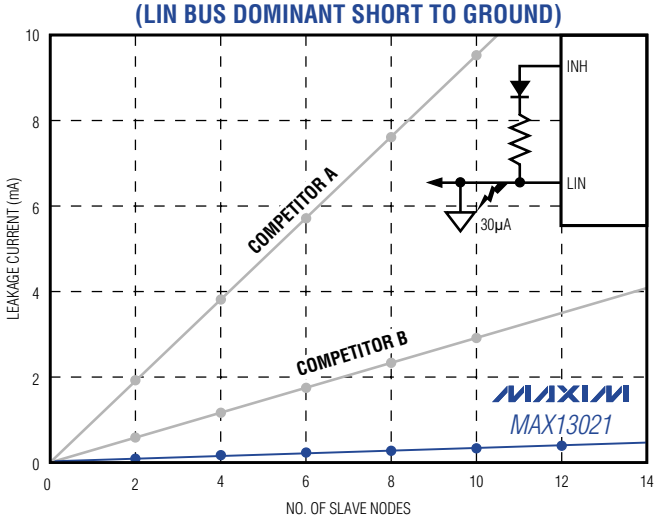
TS 16949 CERTIFIED

CERTIFICATE #40168

PIN COMPATIBLE WITH INDUSTRY STANDARD



FAULT-MODE LEAKAGE CURRENT (LIN BUS DOMINANT SHORT TO GROUND)



Improvements over Competition

- LIN Bus 2.0 Dominant Management (MAX13021)
- 30µA (typ) LIN Bus Short to GND (MAX13021)
- ±60V Maximum Bus Voltage
- 4µA Sleep Current
- Best-in-Class ESD Protection
  - ±12kV Human Body Model
  - ±4kV Contact Discharge on High-Voltage Pins (DN EN 61000-4-2)
- Excellent EMC Performance

Key Specifications

- LIN 1.3 and 2.0 Compliant (MAX13020)
- SAE J2602 Compatible
- IBEE Tested (EMC, Schaffner, ESD)
- Suitable for 12V, 24V, and 42V Applications
- 3.3V and 5V Logic Inputs
- Integrated 30kΩ Resistor for Slave Networks

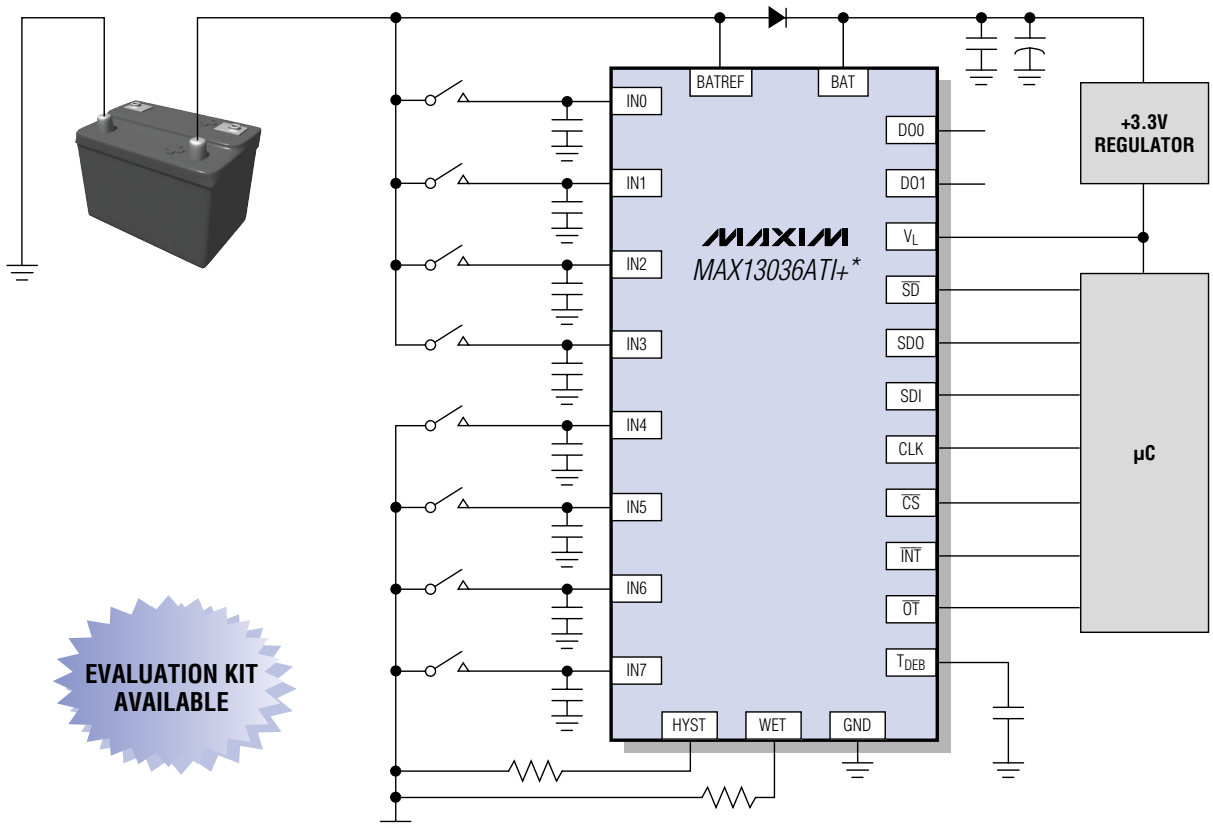
Request a Reliability Report for the MAX13020/MAX13021 at:

www.maxim-ic.com/MAX13020

FUTURE PRODUCT

Automotive Contact Monitor and Level Shifter

The MAX13036* automotive contact monitor and level shifter monitors and debounces eight remote mechanical switches and asserts an interrupt ($\overline{INT}$) if a switch changes state. The state of each switch is sampled through an SPI interface by reading the status register, and any switch can be prohibited from asserting an interrupt by writing to the command register. Four of the switch inputs are intended for ground-connected switches (IN0–IN3), and the other four inputs (IN4–IN7) are programmable in groups of two for either ground-connected or battery-connected switches. Two switch inputs (IN0, IN1) have direct level-shifted outputs (DO0, DO1) for PWM or other timing-based signals. The MAX13036 supplies an adjustable wetting current to each closed switch to clean mechanical switch contacts that are exposed to adverse conditions.



- +6V to +26V Operating Range
- Protected Against Load Dump
- Inputs Withstand Reverse Battery
- ±6kV HBM ESD Protection on Switch Inputs
- Thermal Protection
- Resistor-Adjustable Hysteresis
- Interrupt Output
- 36µA Operating Current in Scan Mode
- Built-In Switch Debounce
- Inputs IN0 and IN1 Programmable as Direct Inputs
- Inputs IN4 to IN7 Programmable to V_{BAT} or GND
- Small, 5mm x 5mm, 28-Pin TQFN-EP Package
- Integrated Voltage Regulator Version Also Available (MAX13037*)

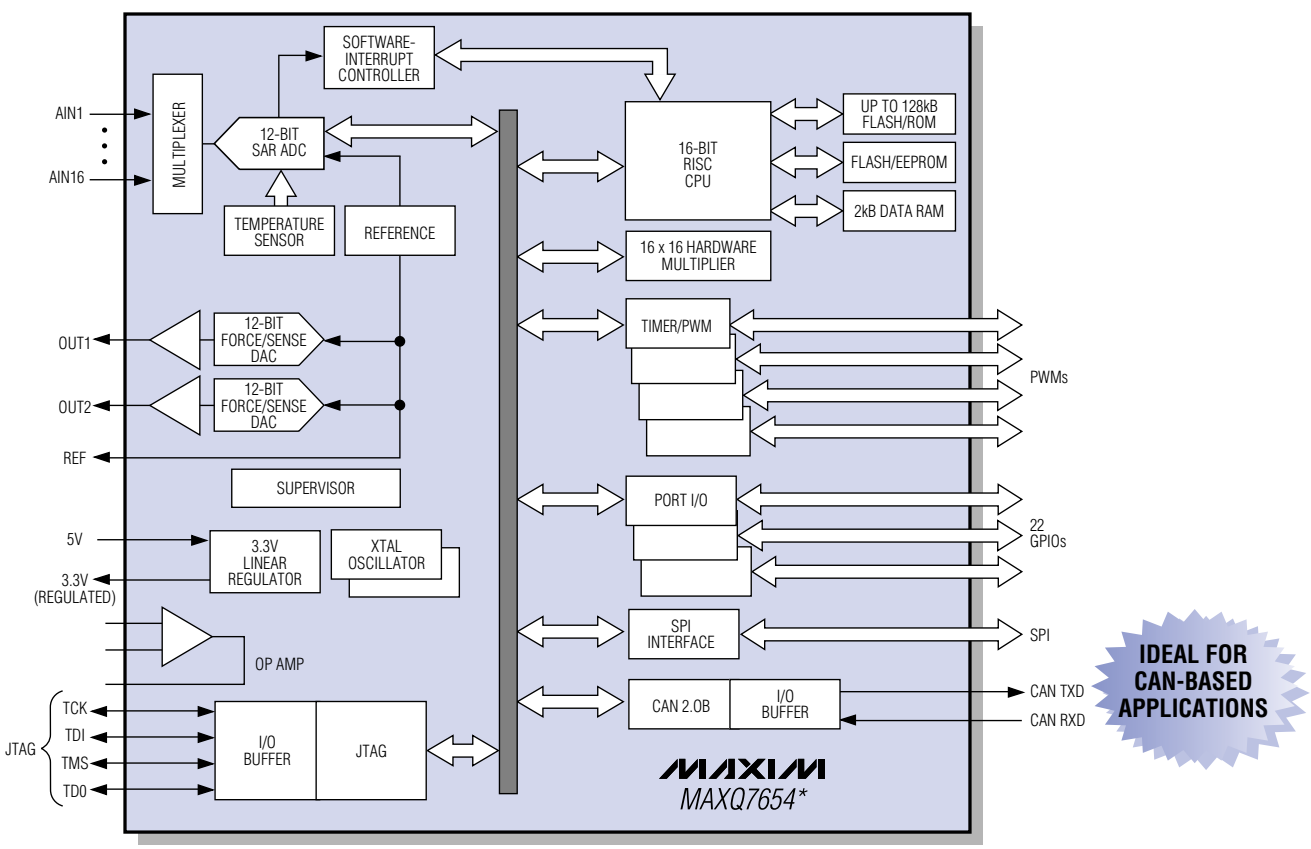
*Future product—contact factory for availability.

FUTURE PRODUCT

16-Bit RISC Microcontroller with 128kB Flash, 12-Bit ADC, 12-Bit DACs, and CAN 2.0B Interface

Provides Precision Automotive Battery Monitoring

The MAXQ7654* is a smart data-acquisition system. This single chip is comprised of a 16-bit, low-power MAXQ20 RISC microcontroller, a 16-channel, 12-bit, 500ksps SAR ADC, and a CAN bus interface. The MAXQ7654's ADC can convert at rates up to 500ksps. The device measures up to 16 external, single-ended signals or up to 8 differential signals. It can also be used to measure the AV_{DD} analog supply voltage without external connections. Other analog functions include: dual 12-bit, buffered voltage-output, force/sense DACs; an uncommitted, low-power op amp; a bandgap-based voltage reference with independent DAC and ADC buffers; local (die) temperature measurement; and remote temperature sensing with a low-cost transistor.

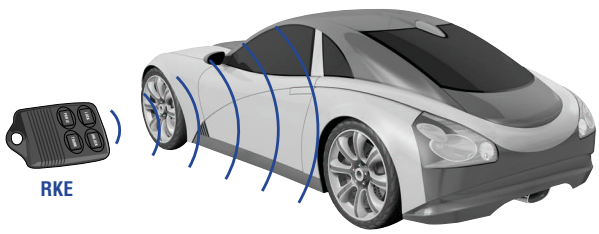


- 16-Channel, 12-Bit, 500ksps ADC
- Two, 12-Bit Force/Sense DACs with Buffered Output
- Bandgap-Based Voltage Reference
- Local/Remote Temperature Sensor
- Low-Power Op Amp
- POR, Supervisor/Brownout Detect
- Internal or External Clock
- Four 8-/16-Bit Timer/Counter/PWMs
- +3.3V, 50mA Linear Regulator

*Future product—contact factory for availability.

DALLAS SEMICONDUCTOR MAXIM

300MHz to 450MHz Transmitters and Receivers Double the Range of Your RKE Systems



Ideal for

- Remote Keyless Entry (RKE) and Remote Start
- RF Remote Controls
- Security Systems
- Tire-Pressure Monitoring System (TPMS)
- Garage-Door Openers

Part	Type	Temp Range (°C)	Power Consumption (mA)	RF Performance at 315MHz	Modulation	Price† ($)
MAX1472	Tx	-40 to +125	5.3 (typ) (ASK at 50% duty cycle)	+10dBm output	ASK	0.96
MAX7044	Tx	-40 to +125	7.7 (typ) (ASK at 50% duty cycle)	+13dBm output	ASK	1.05
MAX1479	Tx	-40 to +125	6.7 (typ) (ASK at 50% duty cycle)	+10dBm output	ASK/FSK	0.97
MAX1470	Rx	-40 to +85	5.5 (typ)	-112dBm with 53dB image rejection	ASK	1.51
MAX1473	Rx	-40 to +85	5.2 (typ)	-114dBm with 50dB image rejection	ASK	1.67
MAX7033	Rx	-40 to +105	5.2 (typ)	-114dBm with 50dB image rejection	ASK	1.69
MAX1471	Rx	-40 to +125	7.0 (typ)	-114dBm (ASK)/-108dBm (FSK) with 45dB image rejection	ASK/FSK	2.39
MAX7042	Rx	-40 to +125	6.2 (typ)	-110dBm with 45dB image rejection	FSK	1.80

Industry's Highest Performance Family of 300MHz to 450MHz Transceivers

Increase Range and Add Two-Way Capabilities to Car Alarms, RF Modules, Remote Controls, Wireless Meters, and Home-Security Systems

Maxim's MAX7030/MAX7031/MAX7032 family of crystal-referenced VHF/UHF transceivers are easy-to-use, high-performance devices that allow quick two-way implementation of one-way systems.

- +10dBm Output Power
- 12mA Tx Current (FSK)
- Automotive Temperature Range (-40°C to +125°C)
- -114dBm (ASK)/-110dBm (FSK) Rx Sensitivity
- 6.1mA Rx Current

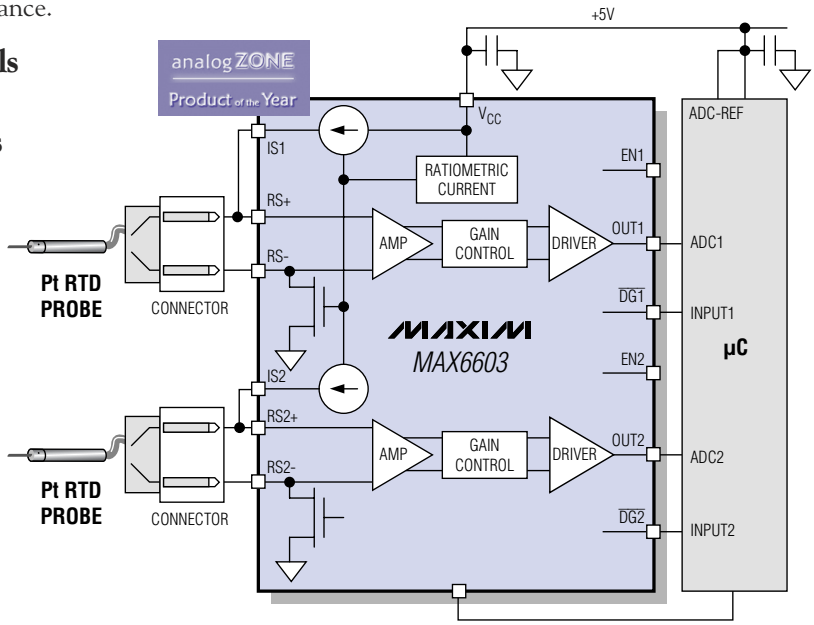
Part	RF (MHz)	Modulation	FSK Deviation (kHz)
MAX7030LATJ	315	ASK	—
MAX7030MATJ	345	ASK	—
MAX7030HATJ	433.92	ASK	—
MAX7031LATJ	308	FSK	±51.4
MAX7031MATJ15	315	FSK	±15.5
MAX7031MATJ50	315	FSK	±49.5
MAX7031HATJ17	433.92	FSK	±17.2
MAX7031HATJ51	433.92	FSK	±51.7
MAX7032	SPI programmable	ASK/FSK	SPI programmable

†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

Industry's First Dual-Channel, Platinum RTD-to-Analog Conditioner Offers ±5kV ESD Protection

The MAX6603 is a small analog conditioner for interfacing resistive temperature devices (RTDs) to microcontrollers. It is targeted for next-generation automotive engine-control systems that utilize exhaust-temperature monitoring for EURO-IV emissions compliance.

- **Amplifies Platinum RTD Signals for ADC Conversion**
- **±5kV ESD Protection at Inputs**
- **Protects CPU from Short-to-Battery Faults Up to 18VDC**
- **Low RTD Excitation Current Minimizes Self-Heating Errors**
- **No Calibration Required**
- **RTD Diagnostics Checks**
- **±5°C (max) High Accuracy from +350°C to +450°C**
- **3.0V to 5.0V Supply Voltage**
- **Small, 8-Pin SO Package**

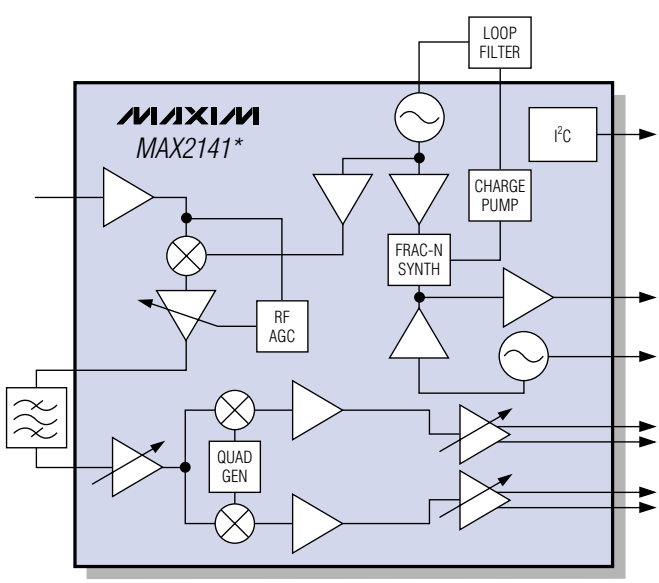


Widest Range of Digital Broadcast Tuners

MAX2141* Enables Low-Power Broadband XM Satellite Radio® Receivers

Maxim's digital radio receivers enable highly integrated, cost-effective designs that are very space efficient. Digital radio is going global, and Maxim has solutions for every part of the world.

The MAX2141 is Maxim's second-generation dual-ensemble receiver featuring low power consumption for XM Satellite Radio applications. It is pin compatible with the industry-standard MAX2140. Also, its much lower heat dissipation allows for placement into an automotive radio head.



Digital Audio Receivers for International Standards

Part	Standard	Region
MAX2140/MAX2141*	SDARS	North America
MAX2161/MAX2162	ISDB-Tsb	Japan/Brazil
MAX2170*	DAB	Europe/Canada

XM Satellite Radio is a registered trademark of XM Satellite Radio, Inc.
*Future product—contact factory for availability.

FUTURE PRODUCT

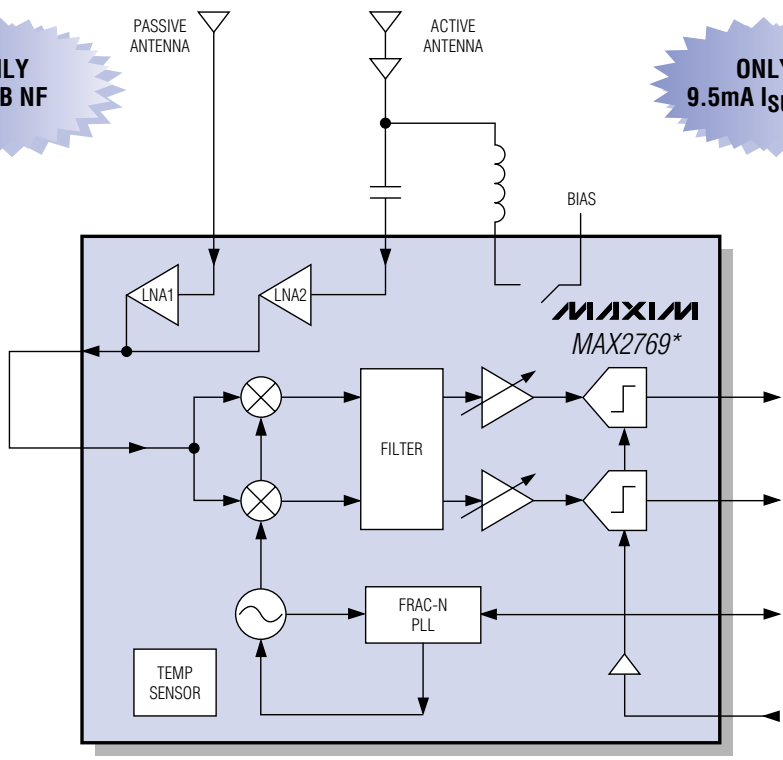
Is Your GPS System Performance Limited by Your RF Front-End?

Improve Your GPS and Galileo Performance and Reduce Cost with the First Fully Programmable, Universal GNSS RF Receiver

The MAX2769* is a single-conversion, low-IF GPS receiver offering a minimum NF of 1.5dB. The integrated ADC output is quantized in 1 or 2 bits for both I and Q channels, or up to 3 bits for the I channel. The fully integrated fractional-N synthesizer and VCO enable programming of the IF between 0 and 8MHz, while operating with any reference frequencies ranging from 8MHz to 44MHz. The MAX2769 includes an integrated active-antenna sensor and a dual-input uncommitted LNA for separate passive- and active-antenna inputs. With its programmable power-savings mode, the MAX2769 consumes as low as 9.5mA. The MAX2769 works with most GPS baseband processors.

ONLY 1.5dB NF

ONLY 9.5mA I_{SUPPLY}



Three Packages Available

- Leadless 28-Pin QFN
- Wafer-Level Packaging (WLP)
- Known-Good Die (KGD)

SAMPLES AVAILABLE

Ideal for

- Cellular E911/E112
- Location-Based Services
- Asset Tracking/Telematics
- Portable Navigation System
- Automotive Navigation

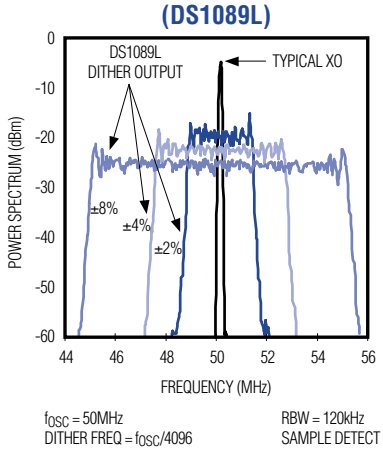
*Future product—contact factory for availability.

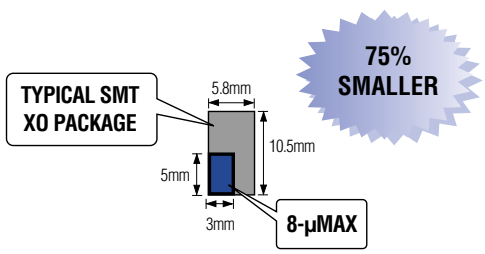
Spread-Spectrum EconOscillators Reduce Peak EMI by Over 20dB

Factory-Trimmed Frequency and Dither Settings Reduce Time to Market

Most applications must meet the stringent radiated-emissions compliance standards established by government agencies. Yet, most crystal oscillators (XOs) do not offer inherent EMI reduction, forcing designers to use expensive shielding, filtering, or PCB-layout techniques to meet these EMI-compliance standards. Our spread-spectrum EconOscillators solve this problem by spreading radiated emissions over a narrow spectrum, thus reducing peak energy at any one frequency. These oscillators are ideal for use as a frequency source for µPs in applications with RS-232, USB, CAN, or LIN peripherals, including automotive infotainment/GPS.

> 20dB EMI IMPROVEMENT OVER XOs (DS1089L)





- **Reduce Peak EMI by Over 20dB**
- **75% Smaller than Typical SMT XO**
- **Lower Active and Standby Power than Typical XO**
- **Fast, Reliable Startup**
- **Less Sensitive to Shock/Vibration than Typical XO**
- **Operates over Automotive Temperature Range**
- **No Price Premium for Higher Frequency Selections**
- **Factory Trimmed, No Programming Required**
- **No External Timing Components Required**

	Part	Min Output Freq (kHz)	Max Output Freq (MHz)	Spread Spectrum	Dither-Mag Range (%)	Dither-Freq Range (f_{OSC}/x)	Power Supply (V)	Temp Range (°C)	Package
	DS1086	260	133	Down	0 to -4	4096	5.0, ±5%	0 to +70	8-SO
	DS1086L	130	66.6	Down	0 to -8	2048 to 8192	2.7 to 3.6	-40 to +85	8-µMAX
	DS1087L	130	66.6	Down	0 to -4	4096	2.7 to 3.6		
	DS1089L	130	66.6	Centered	0 to ±8	2048 to 8192	2.7 to 3.6		
	DS1090	125	8	Centered	0 to ±4	512 to 4096	2.7 to 5.5		
NEW	DS1091L	130	66.6	Centered, down	0 to ±4, 0 to -8	16 to 8192	3.0 to 3.6	-40 to +125	
	DS1094L	31.25	2	Down	0 to -8	128 to 1024	3.0 to 3.6	-40 to +85	

Comprehensive Quality Programs for the Automotive Market

ISO/TS 16949:2002 Certification

Maxim has one of the industry's most rigorous product development, characterization, and release processes combined with preventive and predictive tools to support our continual improvement and zero-defect programs. This is affirmed by our ISO/TS 16949 certification.

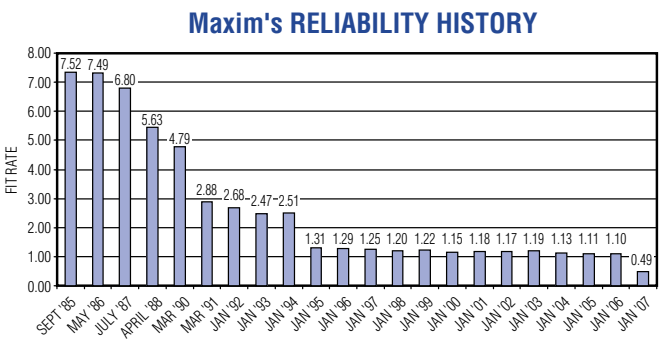
For Our Certificates, Please Visit:
www.maxim-ic.com/qa/quality

AIAG Production Part Approval Process

Maxim is fully compliant to the AIAG automotive requirements. Over 500 customer-specific PPAPs to the 3rd and recently released 4th editions of the AIAG requirements have been delivered. They can be modified to meet any customer requirements in a short cycle.

Improving Product Reliability Through Aggressive Defect Reduction

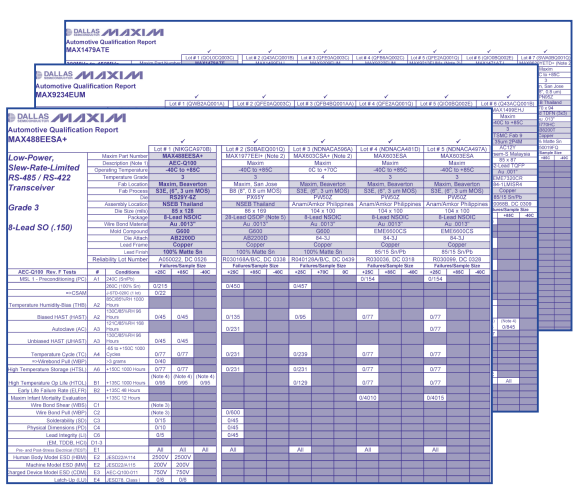
Maxim continuously monitors its products and processes to ensure compliance with established minimum reliability standards and to validate the results of many improvement projects. Reliability testing is done for every part at Maxim and Dallas Semiconductor. Each report is readily accessible and concise. Maxim offers numerous reports on the website, but will also create a report for any product. Very few IC companies even offer reliability reports. The results of our testing can be found on our corporate website.



Product Reliability Reports and AEC-Q100 Reports

- **Lifetime Failure-Rate Estimates**
- **ESD (HBM and CDM)**
- **Latch-Up Sensitivity**
- **Package Construction Information**
- **Temperature-Grade Rated**
- **Process Information**

For Our Reliability Reports, Please Visit:
www.maxim-ic.com/qa/reliability



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I once helped design a digital-guitar amplifier that models the sound of various analog-guitar amplifiers. This amplifier was the first major digital-audio product in what had been an analog-only guitar-amplifier line. The task presented two unusual challenges: generating a synchronized serial-connection clock and correctly programming a flash EPROM.

I used a DSP and a stereo-audio codec that communicated via a synchronous serial port using four connections: data out from DSP to codec, data into DSP from codec, frame synchronization, and a synchronous-clock line that controlled serial-data transfer. I got a sample board up and running with a loopback-audio routine, connected an audio source, and connected a monitor amplifier, but there was no audio coming out of the codec's analog ports. Checking the serial-data connection with an oscilloscope, I found that serial data was running in both directions between the DSP and the codec. The synchronous-clock line and the frame-sync line looked OK.

I wondered whether the external 12-MHz logic clock had to connect to the codec to synchronize with the serial-data-connection clock. Without synchronization, the audio coming out of some codecs would sound like white noise loud enough to damage both loudspeakers and listeners' ears. The data sheet for the device I was using didn't list this requirement. The codec field-application engineer told me that clock synchronization was not a requirement.

A PLL in the DSP converted the 12-MHz clock to higher frequencies, which were then divided down to generate the serial-data-connection clock. The 12-MHz clock came straight from a crystal oscillator that also supplied the 12-MHz clock to the codec. Testing showed that the logic clock and the serial-connection clock were not synchronous but instead sliding asynchronously past each other.

I divided down the 12-MHz logic clock using a CMOS 4040 IC and fed it to both the DSP and the codec. This method removed the PLL in the DSP from the picture and guaranteed that the clocks would synchronize. Upon firing up the board, audio came forth from the codec outputs!

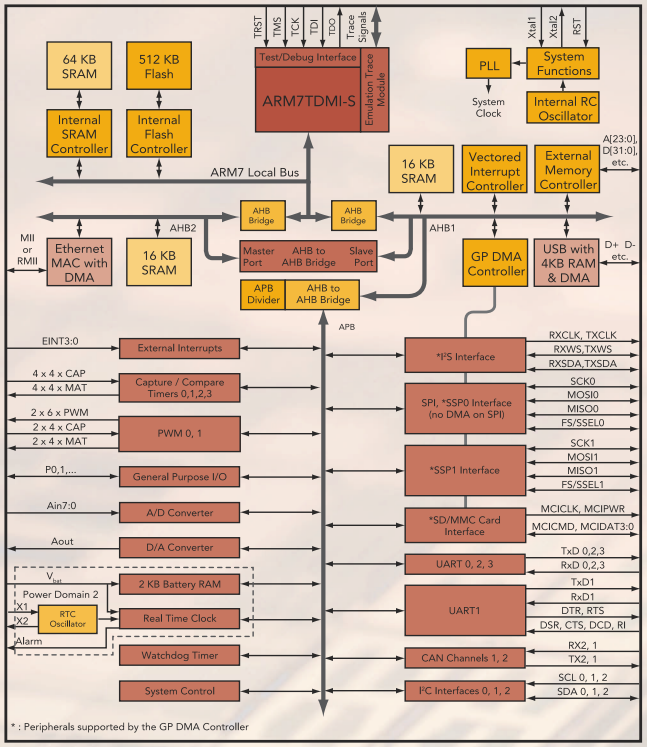
The second challenge came when I was programming flash EPROMs using our EPROM programmer and inserting them into various sample boards. The boards would work fine. I would turn them off and power them back up, and they would be dead. I put one of the flash EPROMs back into the programmer and read back the data that was in the EPROM. The power-up-reset vector, all of the interrupt vectors, and a good portion of the EPROM's contents had changed.

An analog engineer thought the problem might be the power-up sequence at the flash EPROM. We explored that possibility for a while, providing some capacitive delays, but nothing helped. Early EEPROMs required a huge amount of analog-support circuitry, due to the analog-sequencing circuitry necessary to prevent them from altering their contents during power-up, but the device I was using had no such requirements. I found that the flash-EPROM programmer lacked a proper sector-relocking sequence as part of its programming algorithm.

The analog engineer I worked with often said, "It's what you think you know that's holding you back." We thought we knew how to generate a serial-connection clock and that our EPROM programmer worked correctly. We were surprised and wrong on both counts. EDN

Kenneth Ciszewski is a senior project manager for Tech Electronics in St Louis. Like Kenneth, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

DANIEL VASCONCELLOS



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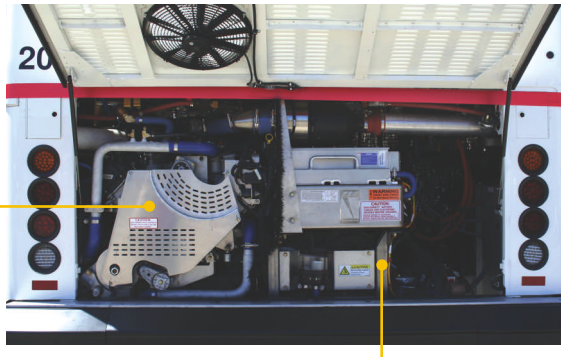
Hybrids mark the end of the stinky city bus

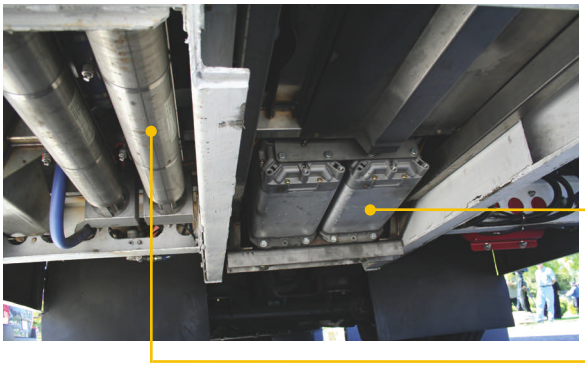
Hybrid-electric designs are well-suited for industrial and commercial vehicles that make frequent starts and stops. The average speed of a city bus is 12 mph, and in New York, it's just 6 mph. Anyone who's been stuck behind a diesel bus in city traffic knows that these vehicles are often serious polluters.

This bus from Complete Coachworks (www.completecoach.com) uses an energy bank of 288 soda-can-sized ultracapacitors from Maxwell Technologies (www.maxwell.com) to power the bus during acceleration and to store the harvested energy during deceleration. Ultracapacitors are lighter and less expensive than batteries, and, unlike batteries, have an unlimited number of charge and discharge cycles. This bus' route is fairly flat: The ultracapacitors need to power it for only about 25 seconds during acceleration; then the gasoline engine provides the steady power.

The power plant for this bus is a Ford Triton V10 gasoline engine, eliminating diesel particulates and producing only about one-fifth of the nitrogen-oxide emissions of a modern standard diesel engine. Conventional buses must use diesel fuel because diesel engines excel at producing the low torque drive that accelerates these heavy vehicles. Because a hybrid's engine needs to provide just steady-state cruise power, not acceleration, this bus can use a cleaner-burning gasoline engine of the size that powers consumer pickup trucks.



The bus' power train, which ISE Corp (www.isecorp.com) designed and built, is a series hybrid design in which there is no direct mechanical connection between the engine and the wheels: The engine powers the generator, which in turn powers the wheel-drive motors.



These two motors drive the wheels. Because there is no direct connection between the wheels and the engine, it's a straightforward design change to select the power plant to fit different driving scenarios, such as using a hydrogen-fuel cell in an area with access to hydrogen fuel.

When the ultracapacitors cannot reclaim all of the braking energy—for example, on downhill grades—braking resistors diffuse the excess energy. Because hybrid buses rely on regenerative braking, they have almost no wear on their brake pads, another pollution-saving feature.

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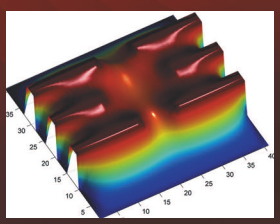

Modeling electric potential in a quantum dot. Contributed by Kim Young-Sang at HYU.

This example available at mathworks.com/ltc

Image: Kim Young-Sang, Jeong HeeJun, Quantum Device Lab, Hanyang Univ. ©2007 The MathWorks, Inc.

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The industry is adopting PCIe in a variety of form factors, such as the Express Card for laptop add-in functions (courtesy PCMCIA Forum).

THE PC'S NEXT-GENERATION INTERNAL PERIPHERAL BUS HAS BEEN QUIETLY OVERTURNING BOTH THE PC AND THE EMBEDDED-COMPUTING INDUSTRIES WITH ITS PERFORMANCE AND EXPANSION POTENTIAL.

PCI Express prompts QUIET EVOLUTION

BY RICHARD A QUINNELL • CONTRIBUTING TECHNICAL EDITOR

Largely unknown to users, the PC industry, with embedded computing following close behind, is in the middle of a quiet shift in technology. The overtaxed PCI (Peripheral Component Interconnect) bus for add-in cards is slowly giving way to the serial PCIe (PCI Express). This change is bringing new capabilities and performance levels to desktop-, laptop-, and embedded-computing systems, but it is also creating short-term design challenges with the technology evolving faster than its adoption.

Now nearly 15 years old, the PCI bus has stretched to its limits. As processor-clock speeds and I/O demands have increased over time, the PCI bus evolved higher speeds and wider buses to boost system performance. But, as with all other parallel-bus structures, problems with the increase in skew and fan-out have also grown with each step in PCI's evolution. The bus years ago reached its limits, prompting the PCISIG (PCI Special Interest Group) to develop a next-generation version that could support legacy applications and software. The PCISIG's answer was PCIe, a switched-serial-bus structure with lower layer hardware that hid this fundamental architectural change from upper layer software.

Links in PCIe are composed of lanes that carry high-speed, bidirectional, serial data point to point within the system. These links have scalable bandwidth and can use one, two, four, eight, 12, or 16 lanes to meet a peripheral's performance needs. The hardware in the PCIe link handles the conversions between parallel and serial forms, the clocking and synchronization of multiple lanes, error detection and correction, and a variety of other tasks that might otherwise require changes in driver, application, and operating-system software. As a result, designers can make a PCIe-bus implementation virtually invisible to the user.

Because of this invisibility, the PC

industry has been quietly switching its board and silicon designs to PCIe without consumers noticing the shift. A look at the PCISIG integrators list for February 2007 gives an indication of how the adoption of PCIe has progressed (**Reference 1**). Nearly a third of the components and silicon IP (intellectual property) on the list address endpoint-controller needs. Another third are graphics devices with native PCIe interfaces from companies such as AMD, ATI Technologies, and Nvidia. Most of the remainder are host- or I/O-root complex switches or bridges to the older PCI and PCI-X buses from companies such as Intel, NEC, PLX Technology, and Via Technologies. Only a handful are peripheral functions, such as Serial ATA or Ethernet controllers with native PCIe interfaces. In the board market, the PCIe integrators list shows nearly 100 graphics-board offerings, whereas other functions each have fewer than a half-dozen instances.

GRAPHICS DOMINATES

This pattern of offerings shows that, for the PC at least, the application driving PCIe adoption has been high-performance graphics. Other high-bandwidth-PC applications, such as Ethernet, Fibre Channel, InfiniBand, and Serial ATA, have also embraced PCIe, but much less enthusiastically. This pattern suggests that the PCI and PCIe buses will continue for many years to be present together in PCs to handle peripheral functions that have been slow to adopt PCIe. A quick look at motherboard offerings available from a local electronics superstore, for instance, shows that almost all PC motherboards have at least one PCIe card slot but still offer several PCI slots.

These surveys of PC offerings, however, do not tell the whole story. The PCMCIA (Personal Computer Memory Card International Association), for example, has also adopted PCIe as an interface for its ExpressCard standard, which it expects to replace CardBus for laptop add-in cards. This adoption extends the applicability of PCIe beyond what the PCISIG has defined, and it is not the only such extension. Among the PCIe silicon-chip offerings is silicon IP from companies such as Cadence, Mentor, and Synopsys for custom chip designs and IP for FPGAs from companies such as Altera, Lattice Semiconductor, and Xilinx. The availability of this IP, especially the cores for FPGAs, indicates a significant market for custom devices and boards with PCIe interfaces, such as the data-acquisition boards from Adlink and National Instruments. Often, these custom designs target the embedded-computing market.

AT A GLANCE

- PCIe (Peripheral Component Interconnect Express) is quietly entering both the PC and embedded-computing markets, lifting the bus-bandwidth limitations of PCI without compromising legacy software.
- Enhancements to the PCIe specification are occurring faster than implementation, creating temporary challenges for system designers.
- Developers must carefully look at motherboard and BIOS selections to ensure that they can achieve maximum performance.
- PCIe cabling offers many new system-expansion opportunities.

PCs' low cost, wide availability, high performance, and immense support infrastructure have long tempted developers to adapt PC standards and technology to embedded-computing applications. When the PCI bus became available, for example, the embedded-system community created CompactPCI, PXI (PCI Extensions for Instrumentation), and the SHB (system-host-board) passive-backplane embedded-computing architectures, among others, based on PCI technology. A new trade organization even arose: the PICMG (PCI Industrial Computer Manufacturers Group).

The same kind of thing has happened with PCIe. Predictably, CompactPCI Express, PXI Express, and SHBe have all adopted the PCIe-bus standard. In addition, new architectures that can use PCIe have arisen. In the demanding telecommunications market, for instance, PICMG has defined the backplane of its ATCA (Advanced Telecommunications Computing Architecture) and its AMC (Advanced Mezzanine Card) modules so that they can use PCIe as an interface. All in all, more than 60 board form factors and a variety of connector configurations with PCIe-bus interfaces are available for industrial and embedded computing.

RAPID EVOLUTION

However, the PCIe specification is evolving faster than designers are implementing. The original PCIe 1.0 specification appeared in 2002, with Version 1.0a arriving a year later and Version 1.1 arriving in 2005. Because the design time for new silicon is typically 18 months or more, many available chip implementations still follow the 1.0a specification, whereas only a few follow 1.1. Fortunately, there are only small differences between the revisions, so they are compatible.

In the meantime, however, the PCISIG has continued to evolve the PCIe specification. Revision 2.0 became available in January 2007, and it offers several significant changes to the specification. One of the most dramatic is an increase in the serial-data rate. The original PCIe specification called for the lanes to communicate at 2.5 Gbps in each direction; PCIe 2.0 doubles that rate to 5 Gbps. To maintain interoperability between the 1.1 and the 2.0 interfaces, the specification has made the speed increase optional and includes an LTSSM (link-training-and-status-state-machine) rate-negotiation feature to identify which speed both ends of a link will support.

Speed increase is not the only new feature of PCIe 2.0, however. In addition to incorporating a number of errata that its developers discovered during the design of Version 1.0a and

You can extend the PCIe bus outside the box using cables, a practice that the PCISIG recently standardized (courtesy Molex).

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Version 1.1 devices, the 2.0 specification has added new functions. One new function is optional programmability and a mandatory disable mechanism for signaling timeouts. This feature helps developers implement designs that may produce longer signal delays than they expect in a motherboard environment. Another optional capability is function-level reset commands, allowing system software to individually reset board functions instead of simply resetting the entire board. A third addition is the use of ACS (access-control service) to support peer-to-peer communications across the PCIe bus.

The PCISIG is not stopping there, however. In February 2007 it released a standard for extending the PCIe bus across a cable (see **sidebar** "Multichassis PCI Express" at the Web version of this article at www.edn.com/070510df1). It is also working on specifications to extend graphics-card power levels to 300W, creating new form factors for add-in cards, and methods to provide I/O virtualization. This virtualization effort is a two-step process to allow a PCIe system to simultaneously behave as several machines using shared hardware. The first step is to define a single-root platform, which allows several operating systems and applications to run on a single hardware platform while appearing as multiple machines to a network. The second step is to define a multiroot structure that allows multiple processors to share peripheral hardware.

PCIe BEYOND THE PC

All these innovations and enhancements to the PCIe specification are greatly expanding its applicability within and beyond the PC market. They are also creating some design concerns that, although they will eventually reach resolution, are becoming challenges for developers trying to apply the technology today. One of the biggest challenges today involves the boot firmware or BIOS, which starts the computing platform after you apply power.

According to Trevor Western, vice president of BIOS engineering at firmware vendor Phoenix Technologies, the challenge centers on how the BIOS should support operating systems and devices that do not offer PCIe or that incorrectly implement it. The backward compatibility to PCI that PCIe offers allows the BIOS developers to at least configure the system as if everything inside were PCI, but this approach is conservative. PCIe has capabilities, such as isochronous transfers, that the standard does not tightly define and that may have variations in implementation. Accessing those capabilities is risky, according to Western. An error in the implementation could lock the system during boot-up.

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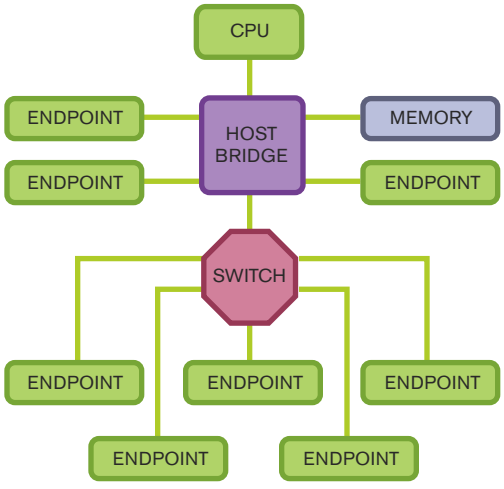
Western also notes that popular operating systems, such as Windows XP and Windows 2000 server software, do not explicitly support the extra features of PCIe, such as hot-plug capability, power management, and MSIs (message-service interrupts). As a result, the BIOS vendors generally disable PCIe functions in computers using these programs unless customers request such support. Some BIOS versions also allow you to turn on the PCIe features during system configuration. Still, developers should be aware of what OS their system uses to avoid disappointment when crafting their peripherals or embedded systems. If the OS or BIOS does not support MSIs, for example, the system reverts to PCI's IRQ (interrupt-request) format and may be unable to attain full PCIe performance.



The PCI Express architecture supports peer-to-peer transfers and a virtually unlimited number of peripheral connections by using a switched-serial-bus structure.

Western points out, however, that this situation is temporary and applies only to older motherboards, BIOS versions, and the computers using this older software. Windows Vista and the forthcoming Longhorn server software do support PCIe's extra capabilities, as will the BIOS of systems designed for them. He also notes that proprietary embedded operating systems and Linux-based systems have had success with PCIe support.

BIOS POSES CHALLENGE

The embedded-computing industry has found other BIOS challenges for PCIe developers, however. One is a problem with enumeration—the allocation of address, memory, and interrupt resources to peripherals during boot-up. Because PCIe is a switched architecture, the BIOS must look through the switch device to locate and identify the peripherals on the other side. Depending on the implementation, this process may cause the BIOS to see more peripherals requesting resources than it can handle, especially if multiple switches are in a cascade. As a result, the system may not enumerate properly.

Another challenge with switch use relates to spread-spectrum clocking. To reduce EMI, the PCIe physical layer can operate with a clock that varies slightly around the nominal 2.5-GHz rate. This variation spreads the energy spectrum of the clock edges into a band around 2.5 GHz, instead of concentrating them at the clock frequency. Spreading the spectrum in this way reduces the peak energy level at any one frequency, keeping system EMI within regulatory limits. Unfortunately, a PCIe switch may not support the use of this technique through its ports, so BIOS vendors typically disable this feature.

The embedded-system community has also become wary of using motherboards designed for desktop or server use. Developers report that some motherboards may have card

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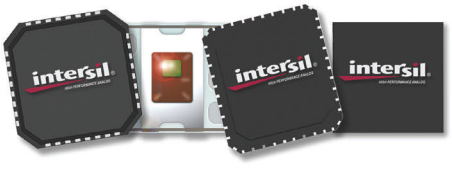

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slots with connectors that handle eight- or 16-lane cards but may route only four lanes for those slots. Having the larger connectors maximizes the possibilities for inserting boards into the system, but failure to route all the lanes causes the motherboard to get less than top performance from high-performance boards.

System designers will continue to face such challenges for the next several years. Standards developers are only now resolving the issues that arose with the adoption of PCIe 1.1, for instance. With PCIe 2.0 having just arrived, no silicon or software is yet available that will give developers access to its features, and experience has not yet revealed the inevitable ambiguities and errata that plague all new specifications. Further, there will be a transition during which both types of PCIe interfaces must work together as vendors migrate their products from one version to the next and customers slowly embrace them.

Still, developers will inevitably face and resolve those challenges. The performance and features available using the PCIe bus are compelling enough to ensure that desktop-, server-, and embedded-computing systems will quickly adopt PCIe. PCIe has been quietly slipping into nearly every type of computing system and will eventually supplant PCI. It just may take a while for it to all settle. EDN

REFERENCE

1 PCI Express Integrators List, www.pcisig.com/developers/compliance_program/integrators_list/pcie/pcie.

FOR MORE INFORMATION

Actel
www.actel.com

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AUTHOR'S BIOGRAPHY

Contributing Technical Editor Richard A Quinnell has been covering technology for more than 15 years after an equally long career as an embedded-system-design engineer.

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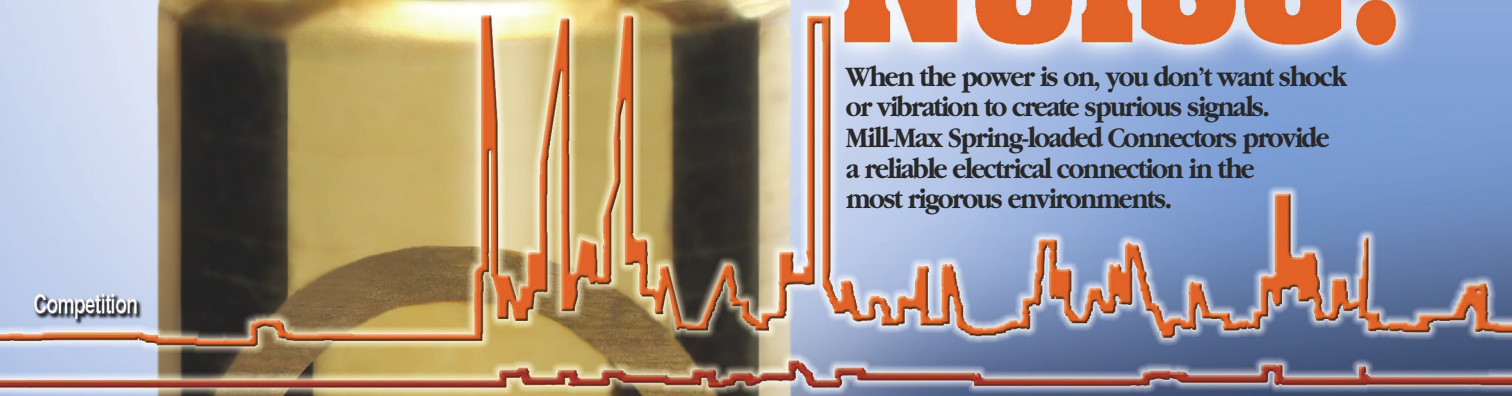

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EDN HANDS-ON PROJECT

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

INTERFACE OVERKILL?

IS eSATA NECESSARY FOR YOUR NEXT SYSTEM DESIGN?

THE EXTERNAL-SATA INTERFACE IS BLAZINGLY FAST, AT LEAST ON PAPER, BUT ITS PERFORMANCE COMES AT A BILL-OF-MATERIALS AND DEVELOPMENT PRICE. SHOULD YOU SHOULDER THE INCREMENTAL EXPENSE IN YOUR NEXT DESIGN, OR WILL A MORE GENERAL-PURPOSE INTERFACE SUFFICE?

High-performance external storage is a godsend for consumers averse to cracking open their gear's enclosure to upgrade its storage capacity or for manufacturers and service providers averse to having their customers tackle such surgery. Looking back over the past few years' worth of interface history, the following chronologically ordered achievements stand out as particularly notable:

• In April 2000, the USB Version 2.0 specification, which added support for 480-Mbps High-Speed mode, a substantial performance boost over its 12-Mbps predecessor, debuted.

• In May 2001, the IEEE 1394 standards committee introduced the Version B specification amendment, adding support for 800-Mbps interface speeds, which were twice as fast as the first-generation IEEE 1394a—that is, FireWire 400. In April 2002, the committee subsequently approved IEEE 1394b, also known as FireWire 800.

• On Aug 23, 2005, the SATA (Serial Advanced Technology Attachment) International Organization announced Version 2.5 of the interface specification after roughly one year of public development. The specification documents, among other things, the eSATA (external-SATA) interface. This standardized eSATA implementation supersedes numerous proprietary external-SATA approaches that predated it (**Reference 1**).

Silicon Image and its partners and competitors in the SATA industry, such as Addonics Technologies, have been talking up eSATA connections since at least mid-2003 (**Reference 2**). And, over the past four years, I've repeatedly wondered why. Granted, transferring small, occasional bursts of data into and out of a hard drive's integrated RAM cache might derive a benefit from SATA's 1.5- to 3-Gbps speeds, as might a cluster of parallel-accessed hard drives, such as a large RAID (redundant-array-of-inexpensive-disks) 0 striped array. But it has always seemed to me that conventional hard-disk drives' 40- to 60-Mbyte/sec sustained-transfer rates would constrain the performance of most applications and most external-storage configurations with just one or a few hard drives. FireWire and USB2, at least on paper, should be equally adept at supporting this per-drive sustained-speed metric, and you might *already* be planning on using one of these more general-purpose interfaces for other peripheral-tethering purposes (**Table A** at www.edn.com/070510cs).

Assuming that your design already has USB2, FireWire, or both, what, if any, justification is there for spending incremental IC, hardware, and software budget to *also* include one or several eSATA ports on the system back panel? Analogously, if you're planning on using FireWire 400, should you upgrade your design to support more costly but backward-compatible—in conjunction with connector-translation dongles—FireWire 800? Those two fundamental questions prompted me to tackle this hands-on project, whose initial results you'll find in this print article and that will live on in cyberspace (see **sidebar** "Online addenda exceed print's storage capacity").

A TOP-NOTCH TEST BED

Benchmarking projects are tricky, because up-front assumptions can heavily influence the outcome. If I select a combination of equipment, software, and usage-model variables that are too specific, my results would be meaningful to only a narrow set of readers. Choose a too-broad set of options, on the other hand, and I end up with a bewildering plethora of outcome data. Peeking ahead at the **tables** of results in this article, you might accurately conclude that I've erred on the side of breadth. Nonetheless, I *still* see plenty of potential external-storage-application scenarios that this project doesn't encompass. It's important, therefore, that you understand my assumptions up-front before proceeding to the conclusions. In that way, you can judge the results from an informed perspective and, if necessary, repeat my testing with altered assumptions that better match your application characteristics.

Note that I conducted my testing on a high-end desktop PC running an up-to-date version of Microsoft's Windows XP Professional (**Table B** at www.edn.com/070510cs and **Figure 1**). I selected Windows XP, as I have in past hands-on projects, because I'm intimately familiar with it and because a diversity of potential benchmarking utilities are available for it. However, if you plan to run an embedded-Linux distribution in your design, for example, you might want to minimally educate yourself on the differences between the two operating systems with respect to storage performance. Consider, as well, taking the next step and using my project as a template for your own Linux-based analysis.

Similarly, consider my choice of an AMD Quad FX system in light of your target-design parameters. I selected this platform for two reasons. First, it encompasses the PCI and PCIe (PCI Express) expansion-interface flavors necessary to minimize any system-bus-induced bottlenecks in testing. Second, I hoped that using dual 3-GHz FX-74 CPUs, each containing two discrete CPU cores, would eliminate any system-processor limits on external-storage performance. However, it's likely that your target design's microprocessor plans are more judicious; if so, keep in mind that software-crunch-

ing bottlenecks elsewhere in the system may suppress any speed disparity between external-storage alternatives that this study reveals.

BENCHMARK ABUNDANCE

In preparing for this project, I surveyed a number of published storage-benchmarking studies from a variety of online and print publications to assess what Windows-based testing suites they used. I came up with a list of approximately 20 synthetic-benchmarking packages (with each package often comprising multiple subutilities) in addition to the wide variety of real-life application-based benchmark sets that commonly find use. Clearly, I'd need to whittle down the options list to a reasonable subset if I ever wanted to finish my work! After much investigation and gnashing of teeth, I settled on two benchmarking utilities—File Systems and Physical Disks—within a testing suite I've used several times in the past, SiSoftware's Sandra.

SiSoftware's documentation states: "File Systems benchmark[s] mounted file systems volumes. [It] shows how your file systems connected to storage adapters and storage hosts compare to other devices in a typical computer. This is not the raw disk performance that other benchmarks test—but the speed of the volume itself that depends on many more factors like file system, operating system cache, position on disk. ... Thus this is the performance you get at the file system level. ... Drive Index: is a composite figure representing an overall performance rating based on the average of the read, write, and seek tests, and file and cache size. The Drive Index is intended to represent drive performance under typical use in a PC. A larger number means better performance. The weighting of the results is not equal; it represents the distribution of different files sizes as used on these devices (obtained through field research).

"Physical Disks benchmark[s] hard disks … the disk itself, not the file system). [It] shows how your physical disks connected to the storage adapters or hosts compare to other disks in a typical computer. As the test measures raw performance it is independent [of] the file system the disk uses and any volumes mounted off the disk. Read Test: Sequential across disk. Write Test: Sequential across disk. Seek Test: random, full stroke. ... Drive Index is a composite figure representing an overall performance rating based on the highest read or write speed across the whole disk ... the higher the better. Access Time is the average time to read a random sector on the disk, analogous to latency response time ... the lower the better."

I configured both utilities to use write-through mode—that is, to bypass Windows' write cache with the intent of more accurately measuring the speed of the external-storage interfaces and their connected storage peripherals. Also, analyzing the benchmarking-results reports provides other useful information: The File Systems test employs a 2-Gbyte test-file size, and both it and the Physical Disks test use overlapped I/O commands with a four-request I/O-queue depth. I left enabled the default-benchmark support for multithreading, commensurate with the four CPU cores in the system.

AT A GLANCE

- The connected system's processing system may heavily influence your storage subsystem's performance, especially if host-side software handles the media management.
- A glut of available benchmark options, although a "good problem," is nonetheless a problem when you're attempting to ascertain concise but meaningful measurement results.
- Interface bottlenecks, either at the system-CPU and core-logic junction or at the storage-peripheral end of the connection chain, may choke the bits traversing an otherwise-speedy configuration.
- Make sure that the reference-storage devices you benchmark mimic the configurations you'll use in your end design.
- Web-site supplements expand on the data sets and conclusions I found in this article.

INTERFACE OPTIONS

Working outward, after considering the CPU and its associated software as potential external-storage-performance bottlenecks, the various system interfaces are next to face scrutiny. The Asus L1N64-SLI WS motherboard within the AMD Quad FX reference system contains Nvidia's nForce 680a SLI (Scalable Link Interface) core-logic chip set, which comprises two MCP

ONLINE ADDENDA EXCEED PRINT'S STORAGE CAPACITY

As usual, page-count limitations precluded me from passing along in this print article some of the interesting information that I uncovered during my research. And, again as usual, the *EDN* Web site provides an alternative publishing venue for this material. Visit the Brian's Brain blog at www.edn.com/briansbrain. There, the posting "AMD's Quad FX: system and strategy" provides additional details on the system I used in my article and analyzes AMD's first plunge into quad-core systems for consumers versus Intel's dual-die, single-package alternative approach. "Analysis downloads and additional results" is the nexus for downloading the multitude of report files and screenshots that my testing generated, as well as the output from the additional planned testing I mention in the article. Speaking of *multitude*, "Benchmark alternatives" will provide links and critiques of other storage-testing suites you might consider for your follow-on studies. "Education: next steps" provides suggestions for further cultivating your external-storage knowledge. And "Share *your* thoughts," as its name implies, provides a forum for you to comment on data from my study that *you* found interesting and to peruse and discuss the observations of your peers. The blog also offers other relevant external-storage postings.

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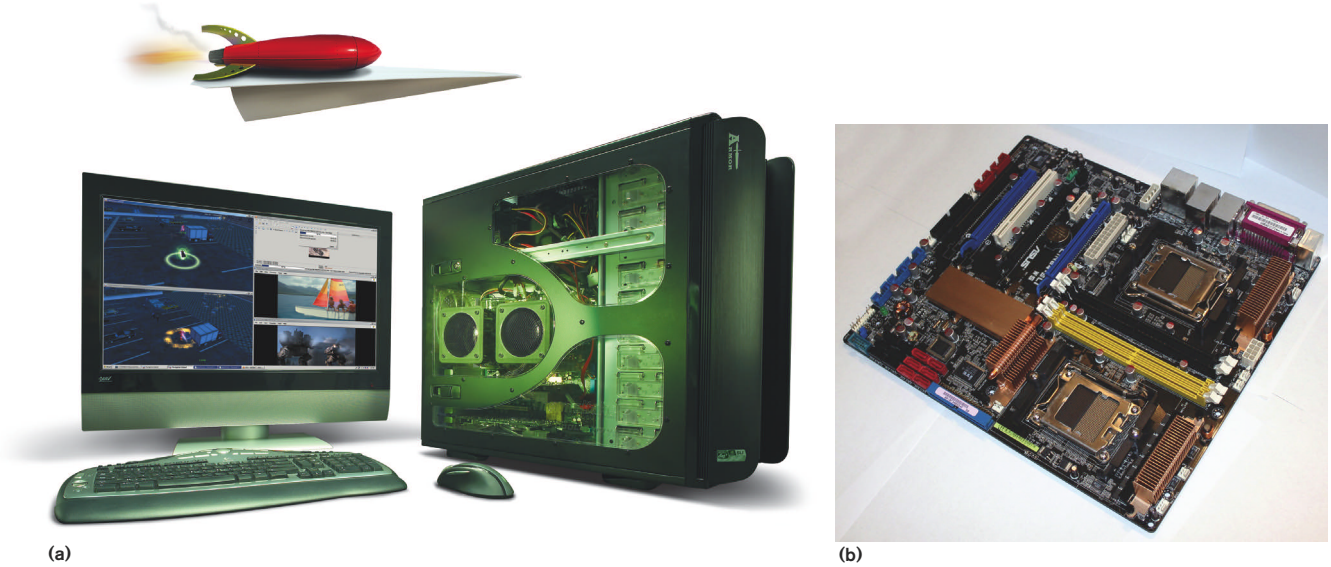

(a) (b)

Figure 1 AMD's Quad FX system (a), containing two dual-core, 3-GHz CPUs (b), provides a speedy and flexible platform for benchmarking various external-storage options.

(media-and-communications-processor) north-bridge chips, each supporting 16- and eight-lane PCIe buses. XFX GeForce 7900 GTX graphics cards running in an SLI configuration populate the motherboard's two 16-lane PCIe connectors; my efforts focused on the "upper" eight-lane PCIe bus along with the motherboard's 32-bit, 33-MHz PCI port (**Table C** at www.edn.com/070510cs). Note that the test system supported Version 1 PCIe speeds.

I employed the motherboard's built-in USB2, FireWire 400, and eSATA capabilities, along with several add-in boards. Asus implemented FireWire 400 and eSATA, respectively, with Via Technologies 6308P and Silicon Image single-lane PCIe Sil3531 transceivers. I tested two FireWire 800 cards—Belkin's 32-bit, 33-MHz F5U23-APL PCI product and NitroAV's one-lane PCIe board. Both PCBs (printed-circuit boards) employ Texas Instruments' TSB82AA2 FireWire 800 IC, revealing that the NitroAV board also contains a PCI-to-PCIe bridge chip.

By press time and despite multiple requests, I was unable to obtain a FireWire 800 reference board from any of the vendors that are supposedly shipping native PCIe ICs. However, because the TSB82AA2 supports both 32- and 64-bit, 33-MHz PCI operation, I anticipated that NitroAV's card might run the PCIe bridge chip in 64-bit PCI mode, thereby boosting performance beyond the capability of the motherboard's 32-bit PCI bus and explaining why I decided to test both FireWire 800 boards.

I also attempted to supplement my testing of the motherboard's native 3-Gbps eSATA capabilities with a Silicon Image eight-lane PCIe add-in board. Its foundation silicon, the 3-Gbps SiI-3124ACBHU, contains a PCI-X interface, so the reference board also includes Intel's PCI-X-to-PCIe bridge. According to Alex Chervet, a marketing manager at Silicon Image, "In a PCIe [eight-lane]-inclusive [Apple] G5 Power Mac, we've clocked over 800 Mbytes/sec sustained performance when [we connected it] to four SV2000s comprising a total of 20 drives." That assertion whetted my appetite to testdrive both available eSATA options.

Unfortunately, I figured out *after* I'd completed my testing that there was a mismatch between the firmware image on the card and the corresponding driver suite I had installed for it and the SATARaid5Manager software. As a result, to date, I've been able to benchmark the Silicon Image SteelVine SV2000 only in its lowest potential performance hard-disk-drive configuration when I tethered it to the SiI3124. For more, visit my blog at www.edn.com/briansbrain, where I hope to post a full suite of testing results on the SiI3124 by the time you read this. I also aspire to post test results for AMCC's 3ware 9650SE-4LPME native PCIe board, which tethers to the Sidecar external-storage peripheral over a four-lane proprietary eSATA bus that AMCC refers to as xSATA.

STORAGE DEVICES

And what storage peripherals will I mate with the external-storage interfaces (**Figure 2**)? (Also see **Table D** at www.edn.com/070510cs.) First up is Seagate's ST3500601XS-RK, which supports 3-Gbps eSATA speeds and contains a single 500-Gbyte hard drive that operates at 7200 rpm and has a 16-Mbyte cache. Maxtor's (now part of Seagate) OneTouch III Turbo Edition includes two 500-Gbyte hard drives operating at 7200 rpm with 16-Mbyte caches. You can arrange these drives in RAID 0 and RAID 1 configurations using the company's OneTouch Manager software. The OneTouch III Turbo Edition offers USB2-, FireWire 400-, and FireWire 800-interface options. Finally, I tested Silicon Image's 3-Gbps SteelVine SV2000, which has five 160-Gbyte hard drives operating at 7200 rpm and with 8-Mbyte caches. The SV2000 can operate in five-partition ("contiguous," in Silicon Image parlance), JBOD (just a bunch of disks, or "concatenated"), RAID 0 ("striped"), RAID 1 ("mirrored"), RAID 1+0—that is, RAID 10 ("mirrored striped"), and, when in a software-based RAID arrangement, RAID 5 ("parity-RAID") configurations.

At first glance, these three products may appear to differ so vastly as to be benchmark-incomparable. Reality, however, isn't nearly so bleak. Note that the two-drive Maxtor unit, which "stripes" its reads and writes across both drives in parallel in its highest performance RAID 0 mode, can also operate in a single-drive-equivalent RAID 1 mode. Similarly, the five-drive SV2000 can also operate as a single-drive (discrete, JBOD, and RAID 1) and dual-drive

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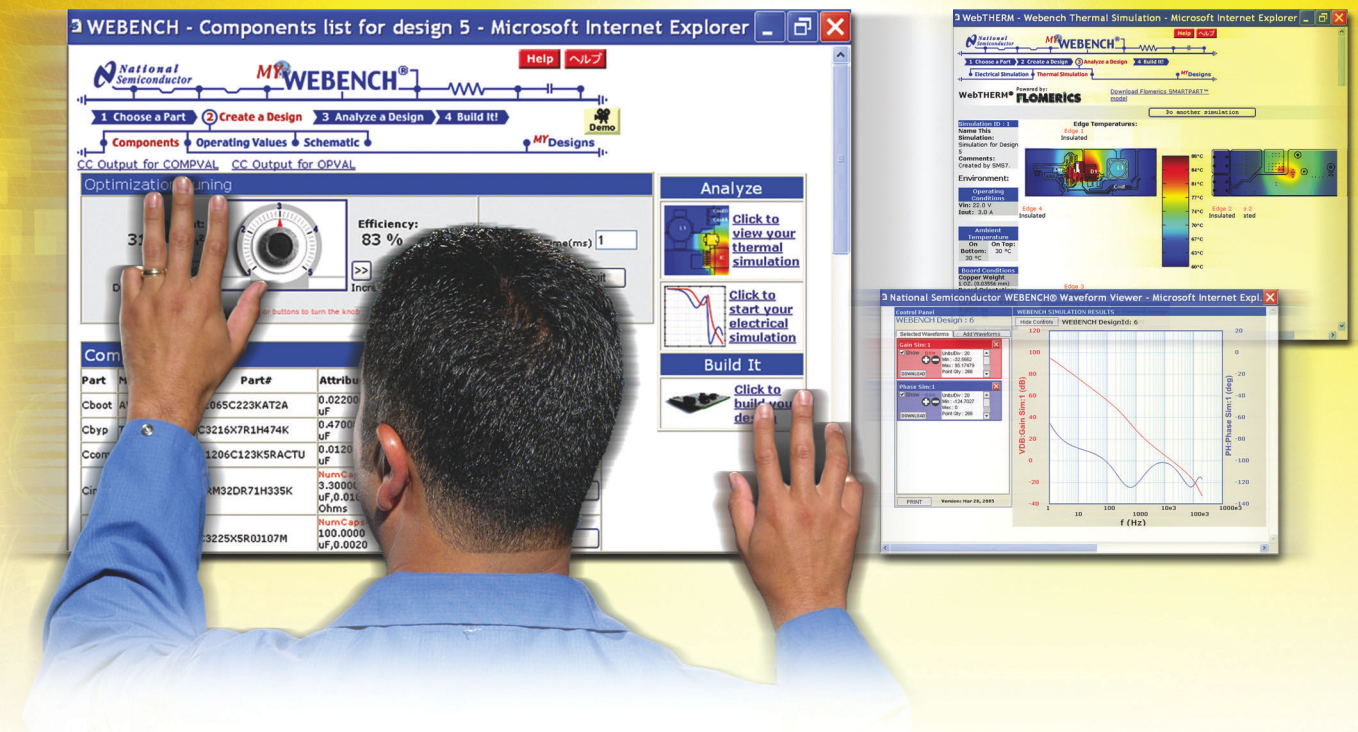

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Figure 2 This article shows test results from Seagate (a), now-Seagate-owned Maxtor (b), and Silicon Image (c) products. Head to the Web for benchmarks of AMCC's quad-lane eSATA setup (d).

(RAID 1+0) equivalent. Keep these common features in mind as you peruse the results.

Keep in mind, too, that RAID configurations incur processing overhead beyond their single-drive counterparts. For mirrored modes, the system needs to write common data to both drives, and it needs to ensure that the parallel data it reads from both drives results in a match. RAID 0 writes a subset of the total information to each drive, and it combines partial-data fetches from each drive during a read operation. RAID 1+0 combines the RAID 0 and RAID 1 requirements, and RAID 5 is even more complex, requiring the calculation of parity information during writes and validation by means of this same parity data during reads.

Silicon Image's SV2000 includes a SiI4726 storage processor whose embedded RISC engine optionally offloads all hard-drive-management tasks, including RAID control, from the host computer's CPUs. A RAID-software stack running on the host computer could—and, with simpler multidrive external-storage peripherals, *does*—accomplish this same function. Which approach produces a higher performance result depends on, among other things, the relative amount of available processing muscle on each side of the eSATA link. To date, I've collated benchmark results for the SV2000 with the SiI4726 in JBOD mode and with all RAID functions consequently implemented in system software through the SATARaid-5Manager. The SV2000's configuration capability, regardless of whether software or the SiI4726 handles the RAID functions, is impressive; users can configure the five hard drives' raw capacity in an infinite variety of ways, encompassing multiple partitions of multiple types and spanning one drive to many drives as well as to a subset of any drive.

The two-drive internal RAID 0 system array, whose stats I include for comparison, comprises two 150-Gbyte Western Digital Raptor hard-disk drives operating at 10,000 rpm and with 16-Mbyte caches. Nvidia's RAID-management utility configures these drives with a 64-kbyte block setting and divides them into two partitions: NTFS (New Technology File System)-formatted drives C and D. The stripe setting for the SV2000 in its striped, mirrored-striped, and parity-RAID configurations was an 8-kbyte chunk. I couldn't determine the stripe size that the Maxtor OneTouch III Turbo Edition employs in RAID 0 mode. I used the default Windows XP cluster size for drives that I formatted in NTFS: Maxtor's OneTouch III Turbo Edition, which was initially formatted as HFS (Hierarchical File System) for use on Apple's OS X; Seagate's ST3500601XSRK, which was in FAT (file-allocation-table) 32 format; and the SV2000, which was unpartitioned and, therefore, unformatted when I received it.

FILE SYSTEMS

I uncovered a few issues during the course of this project; for that reason, I was unable to test some configurations (**Table 1**). Among those problems, as previously mentioned, was the fact that I could not access the SteelVine SV2000 through the SATARaid-5Manager configuration software when it connects to the SiI3124 reference card. For this reason, I could test the SiI3124-and-SV2000 combination with the storage peripheral only in a contiguous configuration. Maxtor's OneTouch Manager also immediately terminated with an error message whenever I tried running it with the PCIe FireWire 800 card plugged into the system, regardless of whether the OneTouch III Turbo Edition was connected to the card. I didn't observe this issue with either the native FireWire 400 ports or the PCI FireWire 800 card, and it precluded me from reconfiguring the OneTouch III Turbo Edition from RAID 0 to RAID 1 mode.

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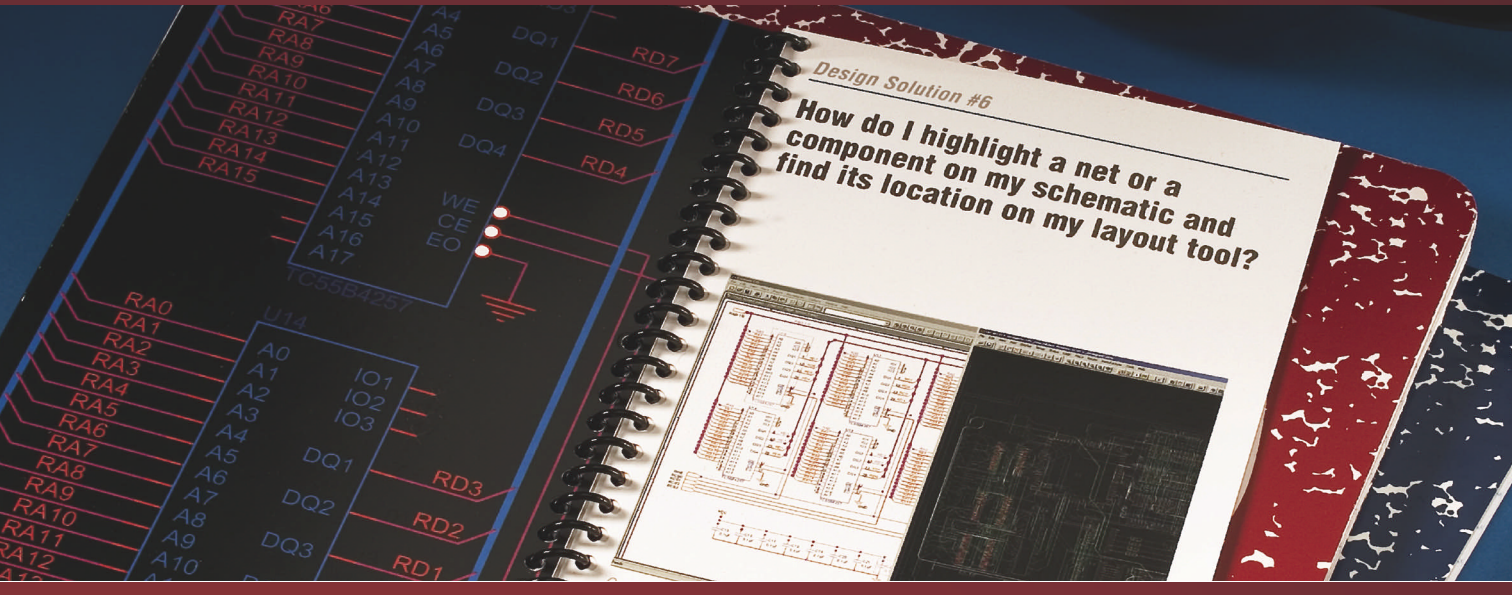

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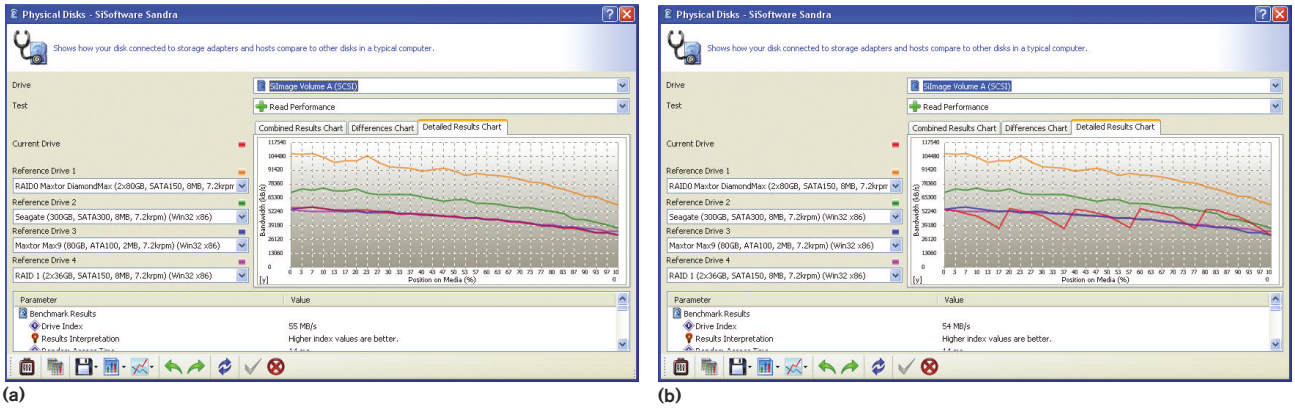

Figure 3 Single-drive- (a) and multidrive-concatenated (b) configurations both reveal varying data-transfer rates across a hard drive's platter.

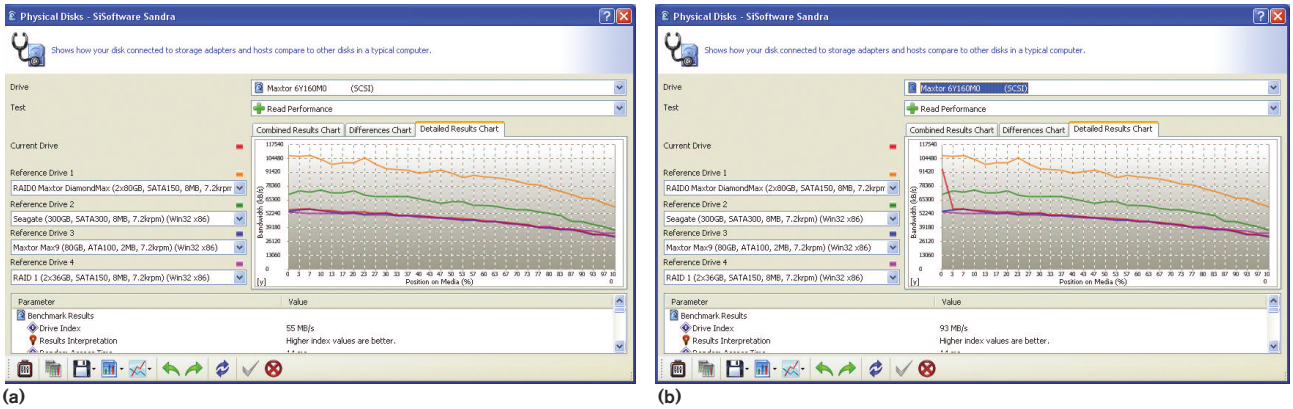

Figure 4 Access-speed profile variability from one run (a) to another (b) suggests, but doesn't definitively prove, benchmark unreliability.

Because my primary motivation was to test the storage peripheral in its fastest possible configuration (RAID 0), thereby potentially maximizing the achievable FireWire 800 bus speed, I didn't focus much effort on resolving or working around the OneTouch Manager issue with the NitroAV card.

When comparing one storage-expansion bus with another, begin by matching up data sets for common-drive-count configurations, such as the RAID 1-configured Maxtor OneTouch III Turbo Edition versus the Seagate ST3500601XS-RK and versus the Silicon Image SV2000 in its concatenated, contiguous, or mirrored modes. Then, see whether reading and writing multiple drives in parallel—the OneTouch III Turbo Edition in RAID 0 mode or the SV2000 in mirrored-striped, parity-RAID, or striped modes, for example—results in a performance increase. These guidelines will help you discern when a given interface, rather than the drive or drives connecting to it, is the performance bottleneck.

Also, note the significant performance impact of running the SV2000 in its parity-RAID (RAID 5) mode. Keep in mind that, in this case, the SiI4726 storage processor handles the parity calculation and confirmation. In contrast, RAID utilities from companies such as Intel with its Matrix Storage Manager and Nvidia with its MediaShield handle this task on the host CPU. Because the SiI4726 storage processor doesn't support RAID 5, the software-based approach I've tested is your only option with this RAID mode. Silicon Image's SteelVine product manager, Jason Green, comments, "I would expect SATARaid5 to run quicker when using the 3124 host-bus adapter. It will be slow on the 3531 link due to the limit of single-lane PCIe." On the other hand, though, note how speedy the SV2000 was in its five-drive RAID 0 striped configuration, approaching and, in some cases, even exceeding the performance of the internal two-drive RAID 0 array. This internal array comprises hard-disk drives with nearly 40% higher rotational speeds and each with twice the RAM cache of its SV2000 equivalent.

USB2's consistently lower read performance than that of FireWire 400 is evident from the results, despite the fact that USB2 has a 20% faster signaling rate. I suspect that higher USB-protocol overhead and USB's need for the host to provide the arbitration and scheduling of transactions are both partially to blame for this discrepancy. The need for the host's actions couples with the relatively simple point-to-point FireWire connections that this benchmarking project uses. These connec-

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tions negate any peer-arbitration overhead that might be present in a more complex FireWire configuration.

PHYSICAL DISKS

In an attempt to better discern the performance potential of various interface-and-drive combinations by operating them in an operating-system-generic fashion, I also ran them through Sandra's Physical Disks benchmark. This portion of the project produced another set of intriguing data, although it brought up at least as many new questions as it solved!

The issues with the NitroAV/One-Touch Manager and SiI3124/SV2000 combinations explain most of the "not-tested" sections of **Table 2**. Two additional omissions this time around both relate to the internal-drive RAID 0 array. I couldn't do a partition-free read test on the array because it had the operating system and applications suite on it. Similarly, Sandra's Physical Disk write test refused to run because it found a valid partition present on the internal-drive set. "For security, so that users don't destroy their data on disks by mistake, the disk to be write-tested must not have any partitions," says SiSoftware spokesman Catalin Adrian Silasi. "The benchmark does not test if the partitions are empty, since each format is different, but whether there are any. Thus, delete any partitions from the disk before benchmarking it."

In many cases, you'll notice a decrease in read and write performance as the drive's head moves across the platter, from the 0 to the 100% position (**Figure 3**). This well-known phenomenon reflects the different linear velocities at a constant rotational speed at various points across the platter's radius, along with different data-storage densities at those same points. If you inspect the output plot of the SV2000 in its concatenated mode, you can clearly see the repeated access-time-degradation pattern as the benchmark cycles from one hard drive to another across the five-drive array.

The Physical Disk data is interesting, but it's dubious enough that I resist drawing any definitive conclusions from it. Look, for example, at the USB2 numbers. How can a bus capable of only 480-Mbps signaling rates generate 83-Mbyte/sec—that is, 664-Mbps—transfer speeds? SiSoftware's Silasi notes, "The test does raw sector reads and writes using I/O Windows functions. Instead of opening a file as the other benchmarks—file system [and] removable storage—do, it opens the disk. The test specifies no buffering, and it reads and writes a multiple of the disk and controller sector size. Although the test specifies no buffering, it is up to the driver to actually honor these requests. As you probably know, when Microsoft introduced Windows

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TABLE 1 FILE SYSTEMS BENCHMARK RESULTS

	Internal SATA		IEEE 1394a (FireWire 400)		USB2		IEEE 1394b (FireWire 800)				eSATA (motherboard)			
							PCI		PCI Express		Seagate		SteelVine	
	C drive	D drive	RAID 0	RAID 1	RAID 0	RAID 1	RAID 0	RAID 1	RAID 0	RAID 1	FAT 32	NTFS	Contiguous (disks 0/1/2/3/4)	Concatenated
Drive index (Mbytes/sec)	130	120	35	34	31	28	70	52	65	Not tested	51	51	50/49/50/50/50	50
Random-access time (msec)	9	9	9	8	10	17	10	8	10	Not tested	7	7	8/8/8/8/8	8
Buffered read (Mbytes/sec)	260	258	30	31	20	14	57	42	57	Not tested	120	120	40/40/40/40/40	40
Sequential read (Mbytes/sec)	168	154	40	38	33	31	88	60	88	Not tested	58	58	57/56/57/57/57	57
Random read (Mbytes/sec)	68	64	29	29	25	21	47	40	47	Not tested	41	42	39/38/38/39/39	39
Buffered write (Mbytes/sec)	83	84	32	31	33	33	62	61	41	Not tested	133	132	80/80/80/80/80	80
Sequential write (Mbytes/sec)	160	147	32	31	33	32	62	58	41	Not tested	58	58	57/56/57/57/57	57
Random write (Mbytes/sec)	100	96	32	31	33	31	61	43	41	Not tested	39	40	42/42/42/43/42	42

Note: eSATA (add-in) concatenated, mirrored (disks 0 and 1/2 and 3), striped (across all five disks), mirrored striped (disks 0 to 3), and parity RAID (across all five disks) were not tested.

XP and Windows 2003, SCSI drives had "worse" write performance—not just in Sandra, but also in other benchmarks. The reason for this [poor performance was that SCSI drives] honored these flags, whereas IDE drivers would buffer regardless of the flag setting. It is possible that the driver for your disk caches and reads ahead for better performance, even when told not to," he says.

Here's another oddity: I would frequently get vastly different read-performance results depending on whether the storage peripheral was partitioned, even though the benchmark was supposedly accessing the device in a non-OS-specific fashion. "The benchmark uses raw-sector I/O with no buffering," says Silasi. "It makes no difference whether the drive is formatted or not. ... [The varying performance depending on the presence or absence of a partition] should not happen." Again, he adds, the driver could cache the data, using system memory it allocates for this purpose, in certain cases, thereby possibly explaining the discrepancy.

The benchmark data is also questionable when it's not repeatable to within a reasonably small percentage, accounting for slight run-to-run variability. I tested the SV2000's read performance in its contiguous mode in the following sequence of steps, each of which I conducted in a drive-by-drive fashion:

1. With no partition and with one-lane PCIe-based eSATA,
2. With no partition and with eight-lane PCIe-based eSATA,

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				eSATA (add-in)		
				Seagate		SteelVine
	Mirrored (disks 0 and 1/2 and 3)	Striped (across all five disks)	Mirrored striped (disks 0 to 3)	Parity RAID (across all five disks)	FAT 32	NTFS	Contiguous (disks 0/1/2/3/4)
	52/52	108	86	50	51	51	50/49/50/50/50
	5/5	6	6	18	7	7	8/8/8/8/8
	48/60	80	122	28	219	219	40/40/40/40/40
	57/57	120	107	79	58	58	57/56/57/57/57
	45/45	72	65	33	41	42	39/38/39/39/39
	63/64	136	70	0.652	140	140	80/80/80/80/80
	56/57	136	70	8	58	58	57/56/57/57/57
	42/42	136	70	0.551	39	39	42/42/42/43/42

TABLE 2 PHYSICAL DISKS BENCHMARK RESULTS

	Internal SATA	IEEE 1394a (FireWire 400)		USB2		IEEE 1394b (FireWire 800)				eSATA (motherboard)			
						PCI		PCI Express		Seagate		SteelVine	
		RAID 0	RAID 1	RAID 0	RAID 1	RAID 0	RAID 1	RAID 0	RAID 1	FAT 32	NTFS	Contiguous (disks 0/1/2/3/4)	Concatenated
Read performance (no partition)													
Drive index (Mbytes/sec)	Not tested	83	38	83	32	83	61	83	Not tested	83	83	55/55/55/55/55	54
Random-access time (msec)	Not tested	17	16	17	15	16	15	18	Not tested	24	24	14/14/14/14/14	14
Speed at position 0%	Not tested	78	36	78	31	78	51	78	Not tested	78	78	55/55/55/55/55	54
Speed at position 33%	Not tested	82	37	82	32	82	51	74	Not tested	82	82	49/50/50/50/50	42
Speed at position 50%	Not tested	66	38	66	32	66	50	80	Not tested	66	66	47/47/47/47/47	47
Speed at position 67%	Not tested	63	37	63	32	61	49	82	Not tested	63	63	42/43/43/43/43	50
Speed at position 100%	Not tested	68	34	68	32	68	36	67	Not tested	68	68	30/30/30/31/31	29
Full-stroke access time (msec)	Not tested	3	2	NR	NR	3	2	3	Not tested	46	46	13/14/14/14/11	3
Read performance (partition)													
Drive index (Mbytes/sec)	150	39	83	32	83	83	83	83	Not tested	58	58	93/93/93/93/93	54
Random-access time (msec)	8	17	17	17	16	17	18	17	Not tested	5	26	14/13/13/14/14	13
Speed at position 0%	142	38	78	31	78	78	78	78	Not tested	50	54	93/93/93/93/93	54
Speed at position 33%	135	39	81	31	81	81	81	82	Not tested	51	51	50/50/50/50/50	42
Speed at position 50%	131	39	82	32	82	82	82	80	Not tested	48	48	47/47/47/47/47	47
Speed at position 67%	125	39	70	31	70	70	70	82	Not tested	43	43	43/43/43/43/43	50
Speed at position 100%	98	39	68	32	68	68	68	67	Not tested	28	28	31/31/31/31/31	29
Full-stroke access time (msec)	3	1	2	1	1	3	2	2	Not tested	28	46	14/12/12/12/12	3
Write performance													
Drive index (Mbytes/sec)	Not tested	83	38	83	32	83	61	83	Not tested	83	83	55/55/55/55/55	87
Random-access time (msec)	Not tested	0	0	0	0	16	0	0	Not tested	8	8	22/21/21/16/21	2
Speed at position 0%	Not tested	78	36	78	32	78	51	78	Not tested	78	78	55/55/55/55/55	87
Speed at position 33%	Not tested	82	37	82	32	82	60	74	Not tested	82	82	50/50/50/50/50	43
Speed at position 50%	Not tested	66	38	66	32	66	60	80	Not tested	66	66	47/47/47/47/47	47
Speed at position 67%	Not tested	63	37	63	32	63	57	82	Not tested	63	63	43/43/43/43/43	50
Speed at position 100%	Not tested	68	34	68	32	68	38	67	Not tested	68	68	30/30/31/31/31	32
Full-stroke access time (msec)	Not tested	NR	NR	NR	NR	NR	NR	NR	Not tested	3	3	1/1/1/1/1	NR

Notes: eSATA (add-in) concatenated, mirrored (disks 0 and 1/2 and 3), striped (across all five disks), mirrored striped (disks 0 to 3), and parity RAID (across all five disks) were not tested.
NR=not reported.

				eSATA (add-in)			
					Seagate		SteelVine
	Mirrored (disks 0 and 1/2 and 3)	Striped (across all five disks)	Mirrored striped (disks 0 to 3)	Parity RAID (across all five disks)	FAT 32	NTFS	Contiguous (disks 0/1/2/3/4)
	52/53	114	147	147	83	83	55/55/93/93/93
	13/13	13	13	14	26	26	14/14/14/14/13
	47/48	109	144	144	78	78	55/55/93/93/93
	42/49	111	142	142	82	82	50/50/50/50/50
	42/47	111	134	134	66	66	47/47/47/47/47
	38/42	114	124	124	63	63	43/43/43/43/43
	29/29	112	98	98	68	68	31/31/31/31/31
	13/13	5	5	5	48	48	13/12/14/13/13
	54/54	138	147	147	58	58	93/93/93/93/93
	14/13	14	13	14	30	30	14/14/13/13/13
	48/54	137	144	144	53	54	93/93/93/93/93
	50/50	132	142	142	51	51	50/50/50/50/50
	47/47	134	134	134	48	48	47/47/47/47/47
	43/43	137	124	124	43	43	43/43/43/43/43
	30/30	132	98	98	28	28	31/31/31/31/31
	12/13	4	5	5	53	43	15/14/10/11/13
	54/54	138	147	147	83	83	55/55/93/93/93
	19/20	1	5	37	8	8	13/14/3/11/13
	48/48	137	144	144	78	78	55/55/93/93/93
	50/50	132	142	142	82	82	50/50/50/50/50
	47/47	134	134	134	66	66	47/47/47/47/47
	43/43	137	124	124	63	63	43/43/43/43/43
	30/30	132	98	98	68	68	31/31/31/31/31
	1/1	NR	NR	17	3	3	1/1/1/1/1

3. With a partition and one-lane PCIe-based eSATA, and

4. With a partition and eight-lane PCIe-based eSATA.

Through Step 1, the five contiguous drives each delivered 55-Mbps read speeds at the 0% head position (**Figure 4**). However, part of the way through Step 2, the 0%-position speed leaped to 93 Mbps, and it stayed there through steps 3 and 4. On a hunch, I went back and retested all five contiguous drives in the Step 1 and Step 2 configurations, and, this time, they all exhibited the 93-Mbps initial-access uptick.

Finally, note that the severe performance penalty that occurred when I ran the SV2000 in its parity-RAID (RAID 5) mode on the File Systems test was not in evidence with the Physical Disks benchmarks.

NEXT STEPS

By the time you read this article, I hope to have made continued progress in a number of areas. Please visit my blog at www.edn.com/briansbrain on *EDN*'s Web site for additional results reflecting this subsequent analysis.

Shortly before wrapping up this article for print, I recalled that Windows XP SP2 at least initially ran 1394a and 1394b FireWire devices at only 100 Mbps (**Reference 3**). I recall that a subsequent OS patch from Windows Update fixed this error, and my benchmark-study results reveal a performance *gain* for FireWire 400 over USB2 and for FireWire 800 over FireWire 400. However, Web research gives inconclusive information on whether I still need to install an obscure Windows "hot fix" to unlock all of FireWire's potential. After I get a definitive ruling on the matter from Microsoft, I'll rerun my FireWire 400 and FireWire 800 tests on the One-Touch III Turbo Edition if necessary.

I plan to rerun my SV2000 tests with the SiI3531, this time with the SteelVine storage appliance's SiI4726 storage processor rather than the AMD FX-74 CPUs handling hard-disk management. I also hope to test the SV2000, in both software- and hardware-based RAID configurations, with the SiI3124 card. The SV2000's performance, especially in striped mode, is impressive, even when you tether it to a one-lane PCIe transceiver. I'd like to see how much faster it could be with an eight-lane PCIe connection.

Speaking of higher eSATA speeds, the AMCC 3ware Sidecar, in conjunction with the 9650SE-4LPME native PCIe board and its quadruple-lane xSATA capabilities, is intriguing. I plan to focus my attention here after tackling the preceding challenges.

SiSoftware's Silasi reports that my erratic test results have spurred him to work on an updated Physical Disks benchmark methodology. "We're working on improving the benchmark to add an offset in subsequent runs," he says. "Basically, instead of reading sectors A, B, C, and D, we're going to read A+block, B+block, and so forth on the second run, thus slightly out of sequence compared to the first run, and similarly alter the pattern again on the third run." I promised him I'd run the benchmark again after he finalizes the update, and I'll report back to both him and you any improvements I encounter.

Finally, I'd like to replace the 7200-rpm hard drives in all four storage peripherals with 10,000-rpm Raptor-drive equivalents and rerun my tests to assess how much faster the results can be in conjunction with Western Digital's SAS (serial-attached SCSI)-threatening speed demons. **EDN**

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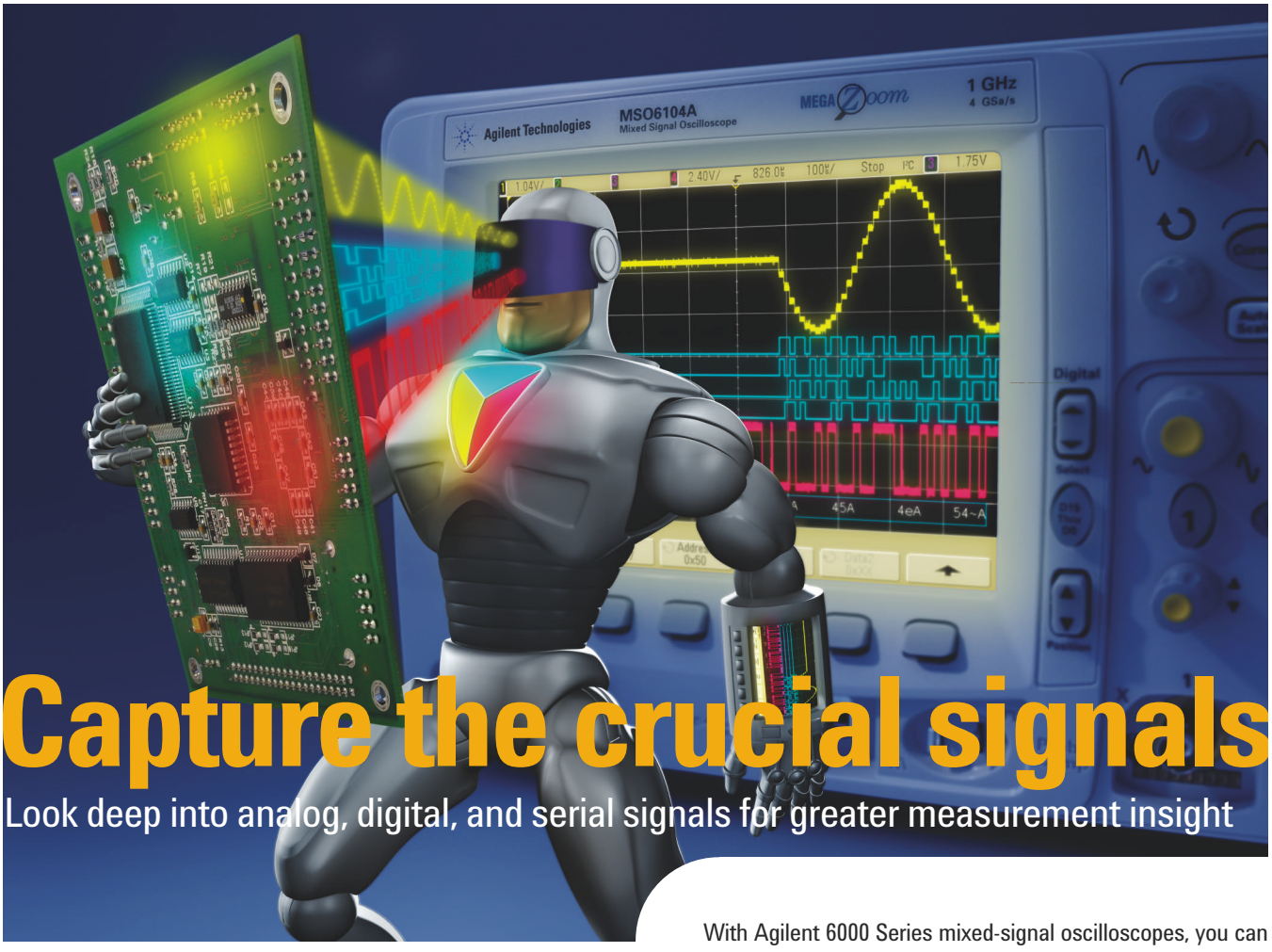

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Extreme low-power design

MODERN IMPLANTABLE MEDICAL DEVICES, SUCH AS PACEMAKERS AND CARDIOVERTER DEFIBRILLATORS, USE AGGRESSIVE POWER-MANAGEMENT TECHNIQUES TO REDUCE SOC POWER.

A typical modern pacemaker may consume on average only a few microamperes of current to achieve long battery life. To meet these low power requirements, engineers use many techniques that may be applicable today to other power-conscious designs. The techniques vary from analog to digital and from circuit to system level, all of which are necessary to keep power to such a minimum.

The first implantable pacemaker in 1959 consisted of a two-transistor blocking-oscillator circuit (**Reference 1**). The 1-Hz oscillator would produce a 2-msec pulse of about 5V that the device would apply directly to the heart with electrodes. A modern pacemaker or ICD (implantable cardioverter defibrillator) has millions of transistors, thanks to VLSI. Physicians can configure hundreds of parameters to meet patients' needs. A pacemaker senses the heart's electrical activity and makes decisions based on its characteristics. It can then deliver appropriate therapy based on programmable values that the physician sets.

Figure 1 depicts a modern pacemaker. The analog chip interfaces with electrodes that go to the heart. It amplifies electrical activity and converts it to digital form. Charge pumps deliver to the electrodes a pacing pulse of varying amplitude and shape. The digital SOC (system on chip) has ROM and RAM for program code and waveform storage. The device requires a large amount of RAM to produce electrocardiograms that a physician can review. The telemetry module allows wireless communication between the implanted device and an external programmer that a physician uses to set operating parameters. A typical pacemaker battery is a 2.8V LiI (lithium-iodine) primary cell.

POWER AND ENERGY

This article concentrates on the power that the digital SOC consumes. Logic circuits can consume power from three sources:

$$P_{TOTAL} = P_{DYNAMIC} + P_{SHORT-CIRCUIT} + P_{STATIC}. \quad (1)$$

Each source requires examination to understand how it contributes to the total power. The dynamic component is the switching power, which is the power the device loses when the circuit capacitances charge and discharge. Typically, this contributor is the largest of the three. You can express the dynamic power by:

$$P_{DYNAMIC} = \frac{\alpha C V^2 f_{CLK}}{2}, \quad (2)$$

where is the activity factor, which is the number of transitions in one clock period and has a value of 0 to 2, and C is the capacitance whose charge is switching at a frequency that the clock frequency determines. For common synchronous circuits, the activity factor is 1, because all transitions occur on only one edge of the clock. All four factors are important, and this article discusses techniques to reduce the effects of each.

Short-circuit power is due to turning on both the NMOS and PMOS elements within a logic gate simultaneously during the switching process. This current is sometimes known as crossover or crowbar current. The slow rise and fall times at the input of logic gates and small load capacitances can exaggerate this condition (**Reference 2**). The good news here is that crossover current is one of the easiest sources of power consumption to control. Typically, this source is less than 10% of the total power dissipated (**Reference 3**). Because this value is so low, this article will not dwell on this source. Instead, it will look at two methods of effectively minimizing crossover current.

Proper gate sizing can minimize short-circuit current. Ensuring that the input rise and fall times are shorter than the output rise and fall times significantly reduces short-circuit current. You can constrain the input-versus-output rise and fall times within the cell-characterization data of the logic cells. It is important to meet these constraints during logic synthesis and at

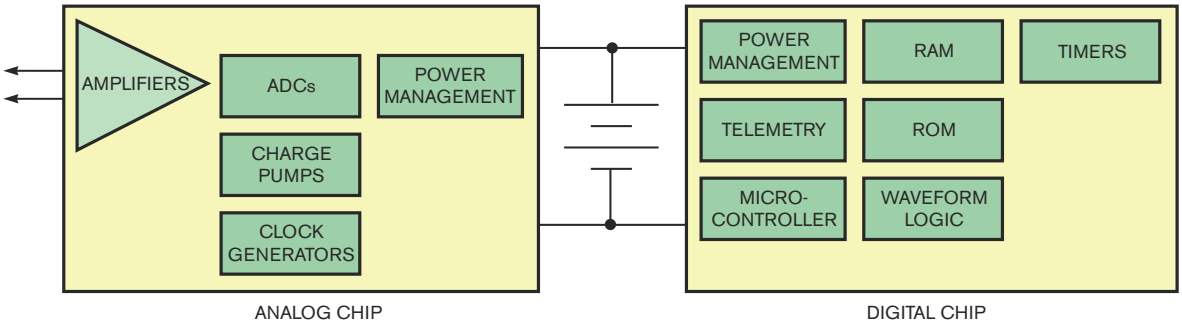

Figure 1 A modern pacemaker comprises two chips to separate analog and digital functions.

the in-place-optimization stage during place and route. With proper cell characterization and design-rule checking, you can keep short-circuit current under control. As you lower the supply voltage to close to the sum of the NMOS and PMOS threshold voltage, short-circuit current is minimal, because the NMOS and the PMOS transistors cannot be simultaneously on.

The circuit consumes static or leakage power while the clocks are stopped. In older CMOS technologies, this power was negligibly small, but, in modern technologies, you can no longer neglect this value. Experts estimate that leakage current increases by a factor of 10 for each process generation (**Reference 4**). For many designs, static power is a significant contributor to power consumption. For modern processes, the main source of this power is subthreshold leakage in the transistor, which is the drain-to-source current flow while the transistor is off.

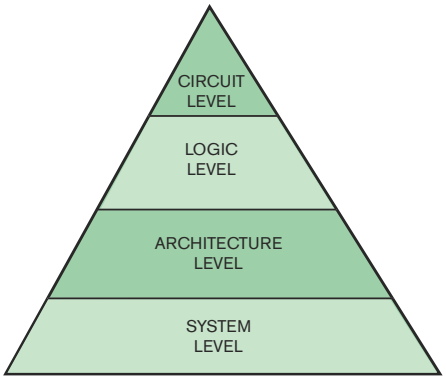

Figure 2 Each stage of the design phase offers varying degrees of power-reduction benefits.

Power reduction can occur at each design stage, bringing varying advantages. The greatest benefit comes at the system level. The least benefit is at the circuit level. You can view these results as a pyramid with power reduction at various stages of design (**Figure 2**). The exact power reduction at each level varies from design to design. As a guideline, the system-level and architecture-level reduction can be orders of magnitude larger than any other level, with the system level offering slightly more benefit. You can achieve power reduction of 10 to 90% at the logic level, and you can expect a reduction of 15 to 20% at the circuit level (**Reference 5**). There are plenty of exceptions to this simplification of power reduction. For example, at the circuit level, varying the thickness of the gate oxide that determines the threshold voltage of the transistor can profoundly affect leakage current. But, in general, this template provides a good way to start thinking about power reduction in an SOC.

One of the most fundamental concepts of conserving power is to shut it off when you don't need it. **Figure 3** depicts this concept: power gating. Power gating is the limit of voltage scaling in which you scale the voltage to zero, thereby reducing the total power to zero. Retaining data is an issue in many cases, so, a typical chip cannot completely lose its voltage supply. But you can shut off sections of the chip when it's not in use. Configuration registers and data-retention flip-flops typically are on a separate uninterrupted power source.

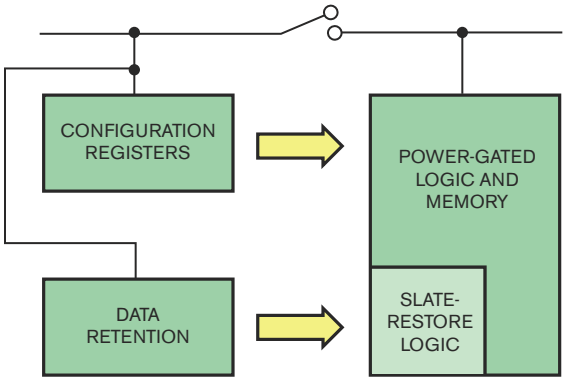

Figure 3 Power gating simply shuts off input voltage when the system does not need it to conserve power.

A close examination of **Equation 2** shows that power scales quadratically as a function of supply voltage; hence, scaling the voltage can greatly impact dynamic power. This concept forms the basis of voltage scaling. From a power-conservation standpoint, running a circuit at the lowest voltage possible is ideal. The lower limit is generally the sum of the NMOS and the PMOS threshold voltages with some noise margin. For this reason, lower geometry IC technology can further lower the voltage. This process is technology-driven voltage scaling. Unfortunately, transistor speed decreases with a decrease in voltage. So you base the final decision of where to set the voltage on circuit performance, reliability, and power consumption. An adjustable on-chip voltage regulator allows you to either statically (based on testing or characterization) or dynamically (based on circuit demand) adjust this voltage.

HARDWARE OR SOFTWARE

High-speed signal-processing applications often implement custom logic to meet the timing requirements. The same is true for very-low-power implementations, often leading to the question of whether to implement a function or an algorithm in hardware or software. There are many trade-offs, such as time, cost of development, configurability, and area, with either approach. For many cases, this question involves whether to choose a serial or a parallel implementation. For a software algorithm, you implement the function in a general-purpose microcontroller unit or a DSP, which involves instruction decoders, instruction fetching, and data fetching to execute the desired function. All operations operate at a higher clock rate (the clock frequency in **Equation 2**) than needed for the actual processing, because a serial process of events must happen before and after the actual computation. A clock can run at a lower rate in a parallel-custom-logic implementation of the same function. In many cases, this rate can be the actual sample rate of the data. This process can lead to a larger but lower power design.

A good example of the hardware-versus-software trade-off is the implementation of a CRC (cyclic-redundancy check). Because software requires so much bit manipulation, this computation can be intense, requiring many clock cycles. In hardware, you can implement a CRC with a simple combination of standard gates and flip-flops. **Reference 6** notes a 53-times reduction in clock cycles with a hardware implementation of a CRC compared with an efficient software implementation of the same function. This reduction, too, would directly translate to a huge reduction of power.

You cannot ignore the impact of software implementation.

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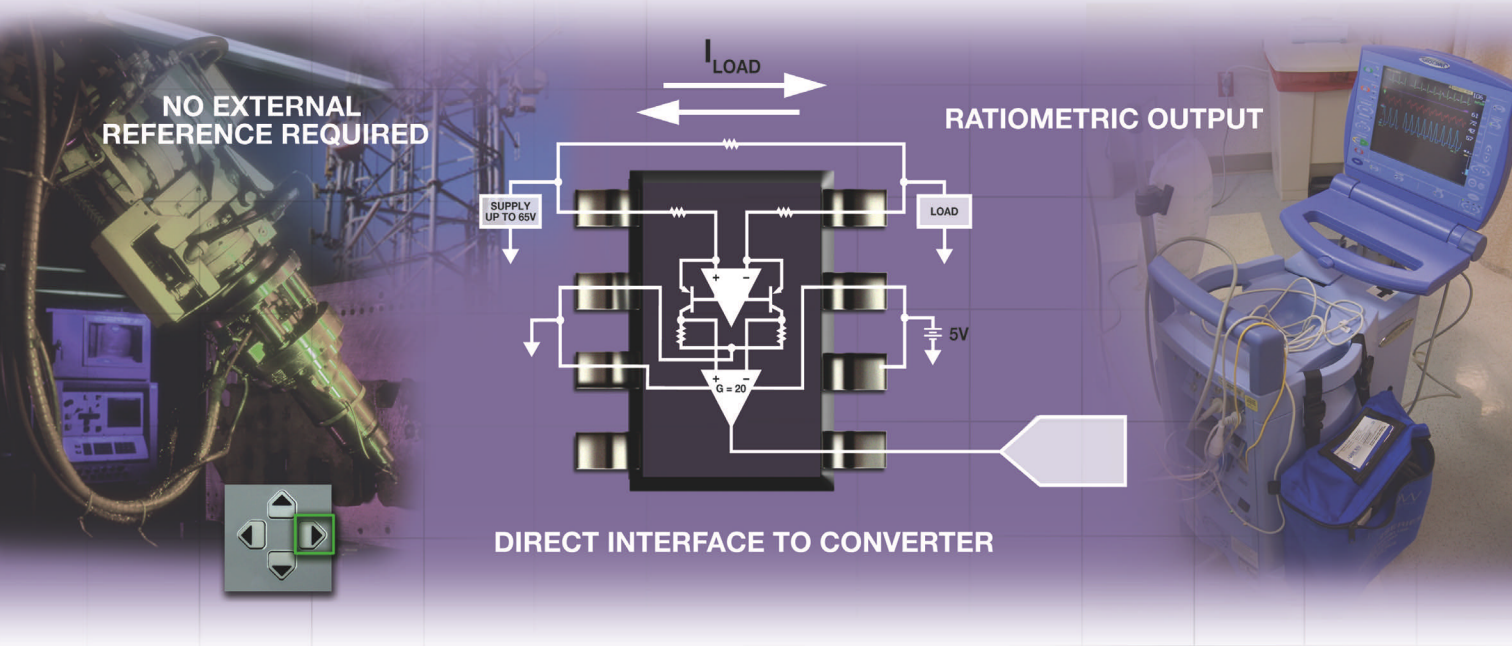

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- 10 ppm/°C typical gain drift
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- 500 kHz bandwidth
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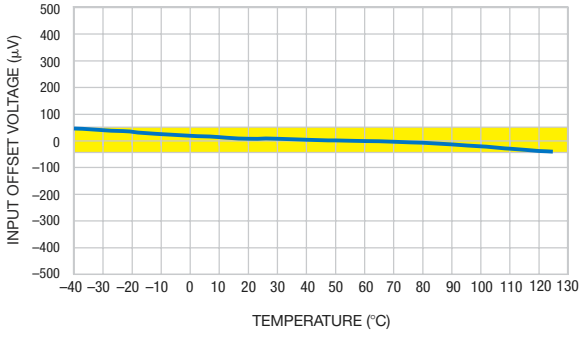

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ANALOG DEVICES

The efficiency at which the system executes a function can largely influence power. Executing a function in as few clock cycles as possible often leads to assembly coding for the best possible results. However, this process is time-consuming and creates processor-specific code.

Accesses to memories can be especially costly. Likewise, a function that relies heavily on instruction fetches, data loads, and data stores can be costly. Code profiling can help analyze and estimate the amount of memory-access activity. As a simple example of the effect of software coding on memory access, consider **Listing 1** (**Reference 7**).

For this example, the code performs f(x) and g(x) on data values A[i] and B[i]. For the example on the left, the processor stores intermediate value B in memory. For the example on the right, the processor does not store B in memory. Aside from being a more concise coding style, the example on the right requires 100 fewer memory-data stores and 100 fewer data loads. Note that coding style as well as compiler transformation can create this kind of inefficiency.

RESOURCE SPLITTING

Reading and writing to system memories can be a large source of SOC-power consumption. Partitioning is a good approach when it comes to memories. This example shows the trade-off of power for area, because a partitioned memory is larger than a nonpartitioned one. Large memories have long word and bit lines, creating large capacitances. Partitioning a memory into smaller instances can be beneficial because a smaller memory consumes less power when something accesses it. Understanding this trade-off can help you decide whether to implement a memory in one or multiple instances. Not all memories are the same. Some memories reduce unnecessary toggling by using a memory cache. Many processors have high rates of associativity with program code. Given this situation, a memory cache can offer power-reduction benefits.

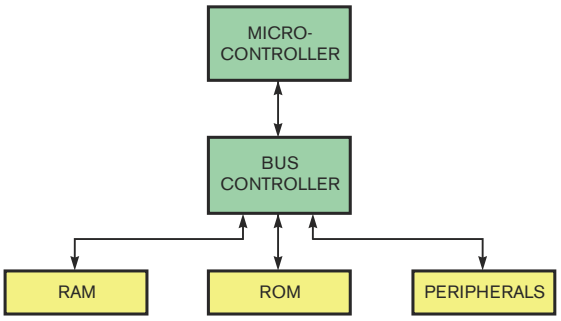

Figure 4 You can split buses to eliminate large capacitances and reduce switching power.

A similar argument holds for multiple buses in a system. One large bus can have a large fan-out and large capacitances that toggle with bus activity. Consider splitting buses to mitigate unwarranted bus switching (**Figure 4**). For example, having separate buses for RAM, ROM, and peripherals reduces the expense of toggling all the devices when communicating to one of them.

The general goal is to reduce unnecessary switching. One of the most effective ways of achieving it is to reduce clocks to the minimum frequency at which they need to run or to shut off clocks when not in use. This objective is the purpose of clock scaling and clock gating. From **Equation 2**, power scales linearly with frequency. Reducing the clock to the minimum it needs to run to achieve performance minimizes the power consumption. For this reason, a low-power circuit may have multiple clock domains, thus allowing circuitry to run only at the minimum frequency. If the clocks synchronize with each other, the designer need not be concerned with clock-domain crossing.

Some EDA tools can automatically insert clock gating, but you must exercise care when employing them. Gated clocks are notorious for creating problems with test insertion and static-timing analysis. Ideally, you gate the clock as close to the source as possible, thereby shutting off as many clock nets as possible. For this reason, clock gating at RTL (register-transfer level) can be the most effective method. A good flow is first to understand where the system is consuming the power in the clock nets and then to find an effective place to gate the clock and choose the appropriate signal for gating. The manual insertion

LISTING 1 CODING SAMPLES

```
for (i=0; i<100; i++) {
    B[i] = f(A[i]);
}
for (i=0; i<100; i++) {
    C[i] = g(B[i]);
}
```

```
for (i=0; i<100; i++) {
    B[i] = f(A[i]);
    C[i] = g(B[i]);
 }
```

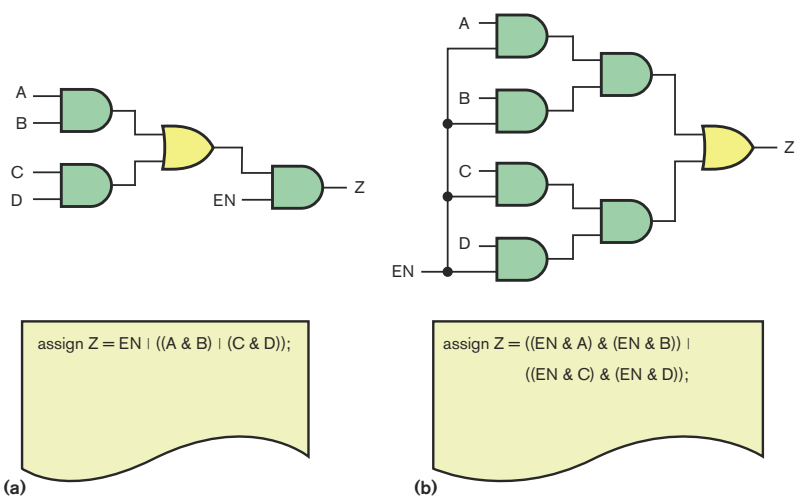

Figure 5 Toggling on operands A, B, C, and D can propagate through two layers of logic before operand EN gates it (a). The logic operand gates the input operands (b).

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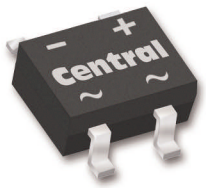
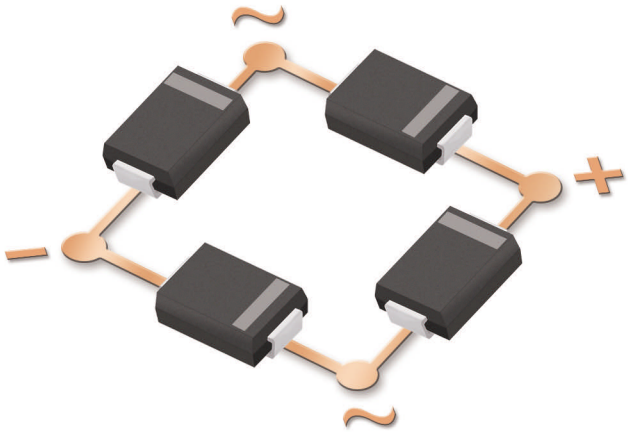


or



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- Laptops
- Data line protection

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- Pb Free and RoHS compliant
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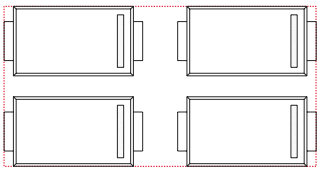
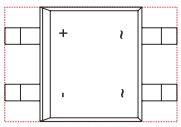


4 SMA packages



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of clock gating is more time-consuming but often leads to better results with fewer gated-clock nets.

Excessive signal toggling is not limited to clock nets. Combinatorial paths can create unnecessary toggling. Consider the following implementations of the same function in **Figure 5**. With the implementation in **Figure 5a**, toggling on operands A, B, C, and D can propagate through two layers of logic before operand EN gates it. With the implementation in **Figure 5b**, the input operand, EN, gates the input operands. Logic synthesis may optimize a circuit according to its constraints. Therefore, the actual logic implementation from a given RTL model may vary. It is always a good approach to evaluate the results after each logic transformation. Also note that some EDA tools during logic synthesis isolate operands either automatically or through RTL-pragma directives (**Reference 8**).

Lesser known techniques have a highly application-specific benefit. For example, sign-magnitude data representation has fewer lines toggling near the zero value than the two's complement (**Reference 9**). Gray coding and bus-inversion encodings may result in fewer lines transitioning on high-capacitance nets, such as address and data buses (**references 10** and **11**). During physical implementation, the goal is to minimize wire length, because it is directly proportional to capacitance. Keeping clock nets as localized as possible with endpoint registers as close as possible to the clock source or gating point is desirable. Good IC floorplanning and a hierarchical place-and-route approach lead to better results.

As noted, threshold voltage can profoundly affect leakage power; the higher the threshold voltage, the lower the leakage. But when performance dictates, the system may require lower-threshold-voltage transistors. As a result, a design can use a mixture of voltage libraries. For paths that easily meet timing constraints, you can use the higher threshold-voltage cells. For timing-critical paths, you can use the lower threshold-voltage cells. Biasing the substrate of the transistor can effectively alter the threshold voltage. In some cases, this technique has produced a 100-times reduction in leakage current (**Reference 12**).

You can use any or all of these techniques to reduce the power of an SOC, such as a pacemaker. Think about all the power sources of **Equation 1** and understand how to control them. You can achieve power reduction at all phases of the design cycle, but you'll see the largest benefit at the system level, so make sure you think about power early. EDN

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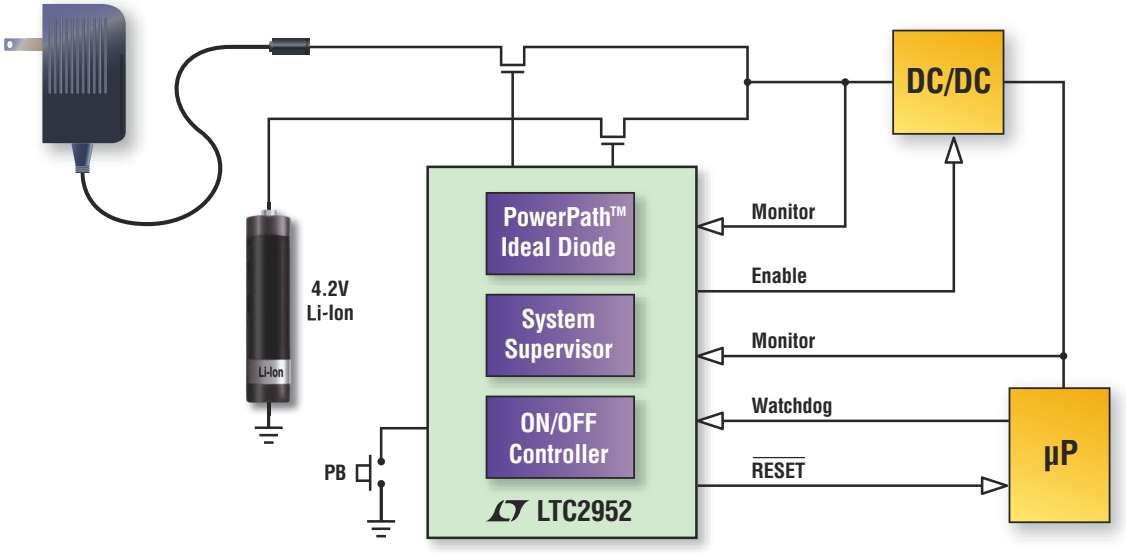
AUTHOR'S BIOGRAPHY

Dean P Andersen is a senior principal engineer at St Jude Medical Inc (Sunnyvale, CA). He holds a bachelor's degree in electrical engineering from San Jose State University and a master's degree in electrical engineering from Stanford University. Andersen's interests are low-power signal processing and embedded systems for medical devices. He enjoys spending time with his kids and biking in the hills around the Silicon Valley.

Simplify PowerPath ON/OFF Control



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Features

Part No.	Supply Voltage (V)	Supply Current	ON Timer	OFF Timer	Kill Timer	Comments	Package
LTC2950	2.7 to 26	6µA	Adj	Adj	1024ms	Active high enable output (LTC2950-1), active low enable output (LTC2950-2)	TSOT-8, DFN-8
LTC2951	2.7 to 26	6µA	128ms	Adj	Adj	Active high enable output (LTC2951-1), active low enable output (LTC2951-2)	TSOT-8, DFN-8
LTC2952	2.7 to 28	25µA	Adj	Adj	Extendable	Push button power path controller with system monitoring	TSSOP-20, QFN-20
LTC2954	2.7 to 26	6µA	Adj	Adj		Interrupt logic for menu driven applications. Active high enable output (LTC2954-1), active low enable output (LTC2954-2)	TSOT-8, DFN-8

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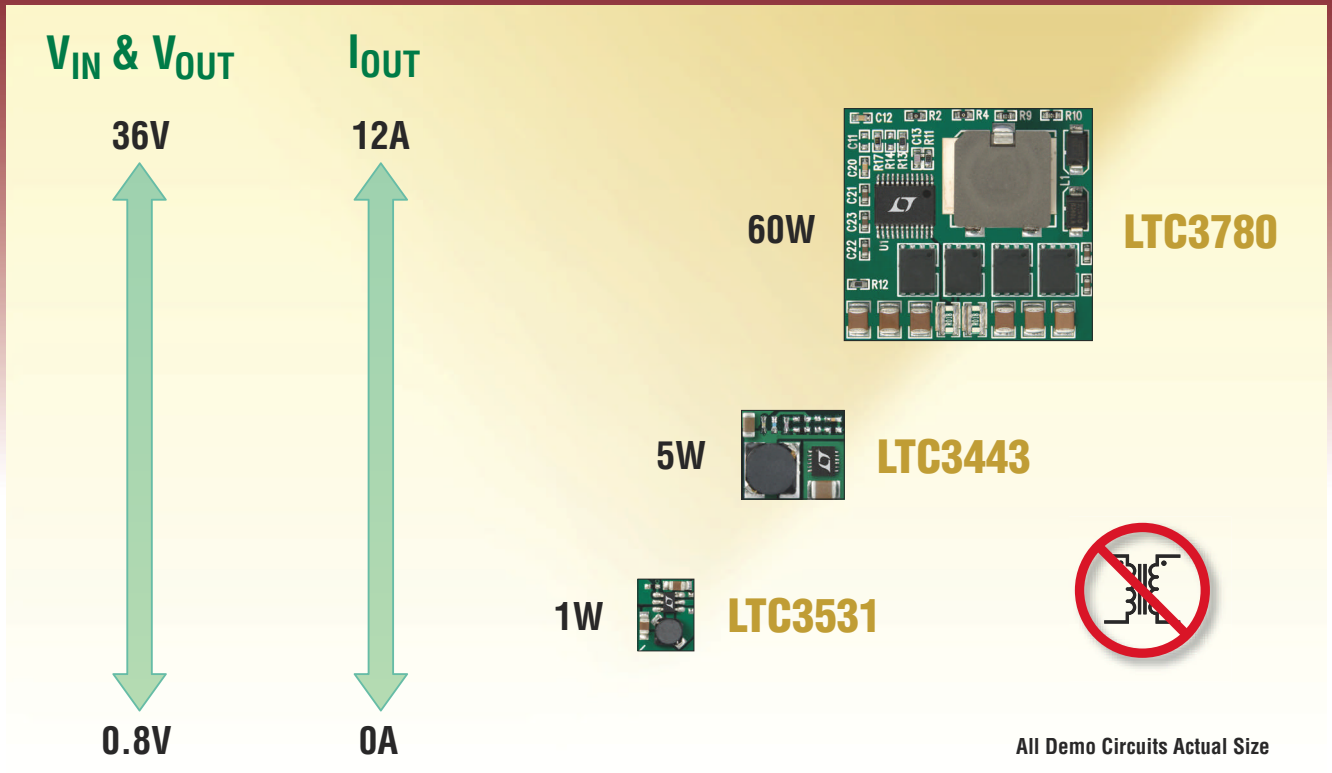

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Buck-Boost Converters

Part No.	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	Frequency	I_Q (µA)	Package
LTC®3531	1.8 to 5.5	2 to 5, 3, 3.3	0.2	500kHz to 1MHz	16	3x3 DFN, ThinSOT™
LTC3532	2.4 to 5.5	2.4 to 5.5	0.5	300kHz to 2MHz	35	3x3 DFN, MSOP-10
LTC3440	2.5 to 5.5	2.5 to 5.5	0.6	300kHz to 2MHz	25	3x3 DFN, MSOP-10
LTC3530	1.8 to 5.5	1.8 to 5.25	0.6	300kHz to 2MHz	40	3x3 DFN, MSOP-10
LTC3441	2.4 to 5.5	2.4 to 5.25	1.2	1MHz	25	3x4 DFN
LTC3442	2.4 to 5.5	2.4 to 5.25	1.2	300kHz to 2MHz	35	3x4 DFN
LTC3443	2.4 to 5.5	2.4 to 5.25	1.2	600kHz	28	3x4 DFN
LTC3785*	2.7 to 10	2.7 to 10	10.0†	100kHz to 1MHz	80	4x4 QFN, SSOP-28
LTC3780	4 to 36	0.8 to 30	12.0†	200kHz to 400kHz	1.5mA	5x5 QFN, SSOP-24

† Depends on MOSFET selection, *Future Product

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DESIGN NOTES

Switching USB Power Manager with PowerPath Control Offers Fastest Charge Time with Lowest Heat – Design Note 415

Dave Simmons

Introduction

Lithium-Ion and Lithium Polymer batteries are common in portable consumer products because of their relatively high energy density—they provide more capacity than other available chemistries within given size and weight constraints. USB battery charging is also becoming commonplace, as many portable devices require frequent interfacing with a PC for data transfer.

As portable products become more complex, the need for higher capacity batteries increases, with a corresponding need for more advanced battery chargers. Larger batteries require either higher charging current or additional time to charge to their full capacity. Most consumers look for shorter charge times, so increasing the charge current seems obviously preferable, but increasing charge current presents two major problems. First, with a linear charger, increased current creates additional power dissipation (i.e., heat). Second, the charger must limit the current drawn from the 5V USB bus to either 100mA (500mW) or 500mA (2.5W) depending on the mode that the host controller has negotiated.

PowerPath™ Controllers Deliver More Power to the System Load

There are two methods commonly used to extract power from a USB port. The first method uses a current limited battery charger directly between the USB port and the battery. This is referred to as a Battery Fed System because the system load is powered directly from the battery. Available power is given by $I_{USB} \bullet V_{BAT}$ because V_{BAT} is the only voltage available to the system load. When the battery is low, nearly half of the available power can be lost within the linear battery charger element. In low battery voltage protection mode, as little as 5% of the available power may be usable.

The second method develops an intermediate voltage between the USB port and the battery. This intermediate voltage bus topology is referred to as a PowerPath System. In PowerPath ICs, a current limited switch is placed between the USB port and the intermediate volt-

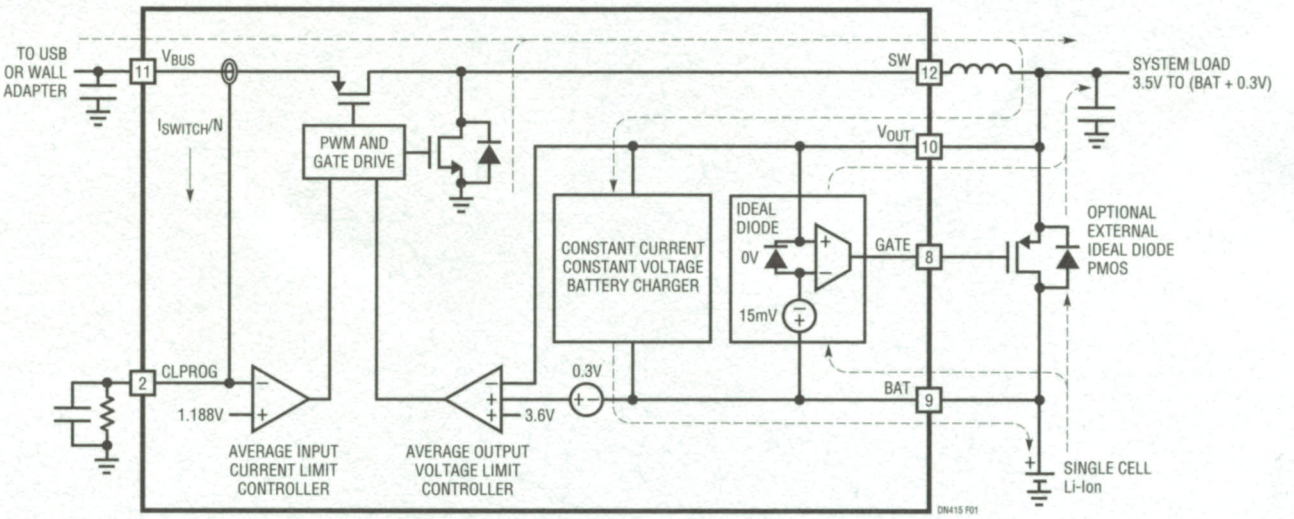

Figure 1. LTC4088 PowerPath Topology

age. The intermediate voltage, V_{OUT}, then powers both a linear battery charger as well as the entire portable product. By using the intermediate voltage bus topology, the battery is decoupled from the system load and charging can be carried out opportunistically. During charging with a PowerPath system, the full 2.5W from the USB port is made available to the system load as long as the input current limit has not been exceeded. In this case V_{OUT} is just under the input voltage (5V for example). However, since the battery voltage is much lower than the 5V input, significant power is still lost to the linear battery charger element.

LTC4088 Makes Charging More Efficient

The LTC®4088 replaces the current limited switch in traditional PowerPath systems with a 2.25MHz buck mode synchronous switching regulator, as shown in Figure 1. The intermediate voltage, V_{OUT}, is regulated to just above the battery voltage. Because power is conserved in a switching regulator, the available output current is higher than the input current.

LTC4088 Reduces USB Charge Time

This additional current can be used to power the portable product and charge the battery more quickly. Figure 2 shows the typical improvement in charge current versus a linear charger when powered from a 500mA USB port.

LTC4088 Eases Thermal Constraints

The second benefit of the switching regulator is heat reduction. Power lost by inefficient charging can cause the external case of a portable product to become uncomfortably warm, and in extreme cases, it can cause thermal limiting of the battery charger. Figure 3 shows the typical efficiency and power savings of the LTC4088 relative to a linear charger when connected to a 500mA USB port.

The LTC4088 also includes a mode designed for use with AC powered wall adapters, in which the maximum input current is limited to 1A. Available current to the system load and battery charger ranges somewhere between 1A and 1.8A, depending on the battery voltage. Many higher capacity batteries are capable of charging at these higher rates, but with a volt or more difference between the wall adapter and the battery, the accompanying dissipative heating cannot be tolerated. Until now, these applications simply had to settle for a lower than optimal charge rate, and accompanying longer charge time.

Conclusion

The LTC4088 offers a dramatic advancement in battery charging and power path management technology, with its reduction in both heat generation and battery charge time. Designed specifically for portable applications, its high switching frequency and internal compensation require only a small inductor and output capacitor. Only the LTC4088's unique topology of a buck mode switching regulator working in tandem with a linear battery charger can give this unparalleled performance.

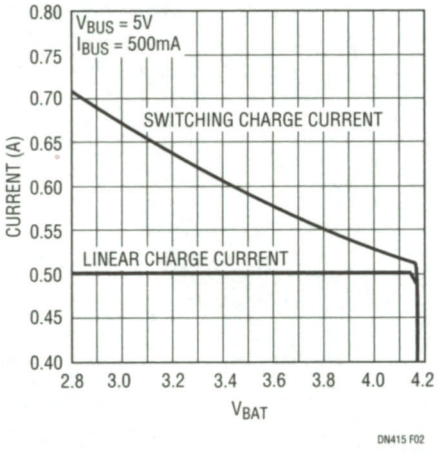

Figure 2. Typical Charge Current for LTC4088 vs Linear Charger When Powered from a 500mA USB Port

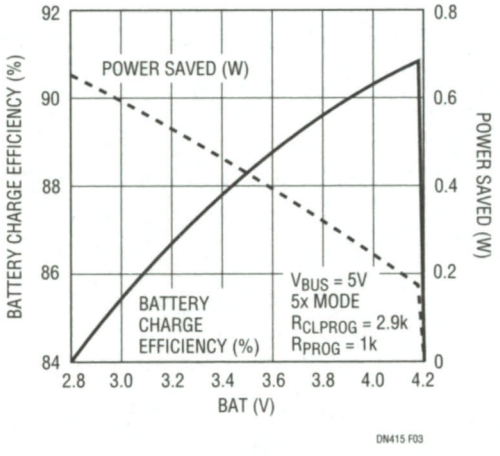

Figure 3. Battery Charger Efficiency and Power Savings Relative to a Linear Charger When Charging from a USB Port

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READERS SOLVE DESIGN PROBLEMS

Microcontroller functions as voltmeter

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

The circuit in **Figure 1** is an extension of a previous Design Idea on how to use an analog input in a microcontroller lacking a built-in ADC, and it takes into account tricks from another Design Idea on how to drive a seven-segment LED display without external switching transistors (**references 1** and **2**). This circuit adds a serial link and needs only a twisted pair to send each measurement to a compatible PC. The serial link was tested using a Microsoft (www.microsoft.com) Hyper Terminal configured at 115,200 baud; at 8, N, and 1; and with no flow control.

Briefly, the software drives one seven-segment LED display at a time, through lines RA0 and RB7. Setting the RA0 output high and RB7 as the

DIs Inside

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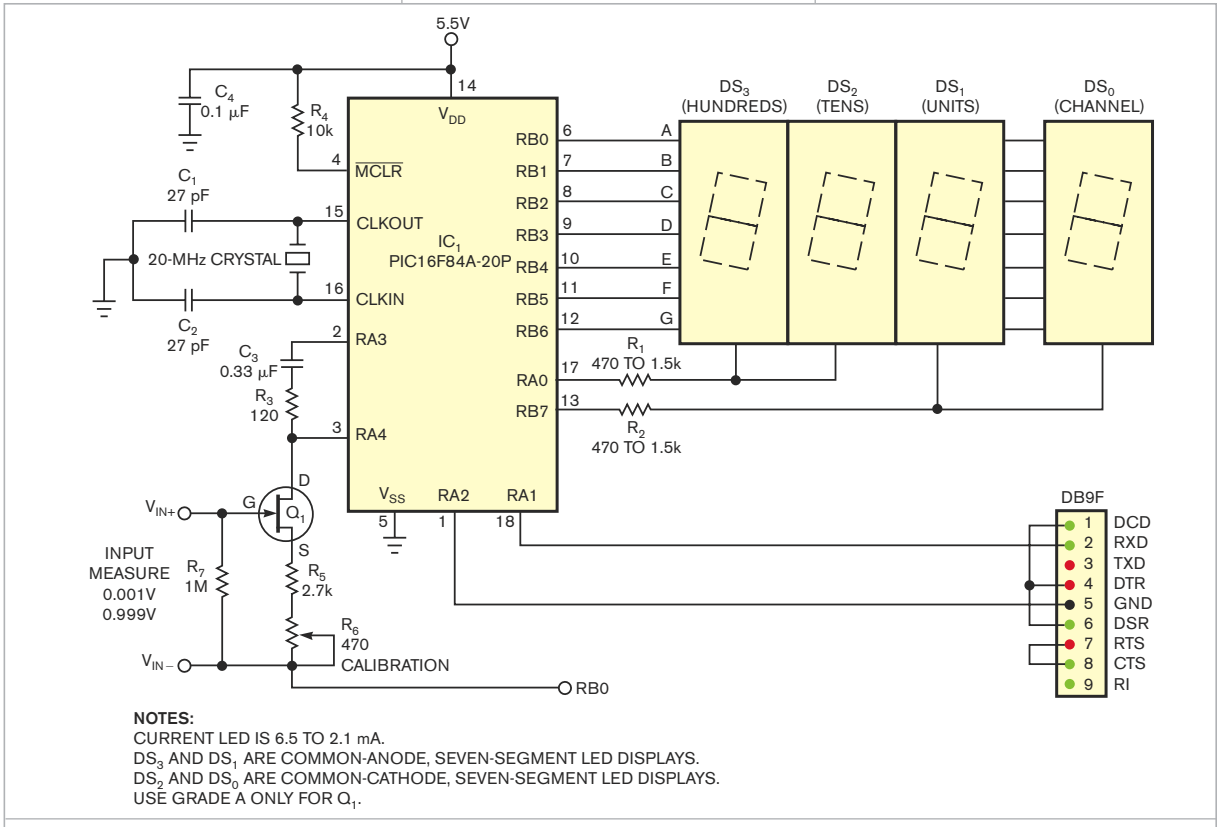

NOTES:
CURRENT LED IS 6.5 TO 2.1 mA.
DS_3 AND DS_1 ARE COMMON-ANODE, SEVEN-SEGMENT LED DISPLAYS.
DS_2 AND DS_0 ARE COMMON-CATHODE, SEVEN-SEGMENT LED DISPLAYS.
USE GRADE A ONLY FOR Q_1.

Figure 1 By using common-anode and common-cathode, seven-segment LED displays, the I/O ports of a microcontroller can drive the displays without using additional external components.

input activates common-anode display DS_3. Setting the RA0 output low and RB7 as the input activates common-cathode display DS_2. With RA0 as the input, setting the RB7 output high activates common-anode display DS_1, and, with RA0 as the input, setting the RB7 output low activates common-cathode display DS_0. While successively activating one display, only one line, RB0 to RB6, is configured as an output to drive one LED segment. This design no longer is limited to a V_{DD} of 3V or lower, because LEDs inversely connect in parallel, so the forward voltage of one diode limits the reverse voltage of the other. Using a red-diode display requires 1.6V.

Figure 2 illustrates the new aspects of this Design Idea. Q_1, R_5, and R_6 act as an equivalent variable resistor, R_X, which charges capacitor C_3. Instead of pulling R_X to ground, just connect it to one I/O—RB0, for example—of the microcontroller. If RB0 is an output with a low state, then the first analog channel activates, and the measure subroutine counts pulses of charge as high as 66% of V_{DD}; then, a look-up table converts this time delay to a three-digit millivolt value. To expand the number of analog inputs, you can connect as many as seven variable-resistor circuits in a parallel configuration—that is, each one connects between C_3 and one I/O line, RB1 through RB7. Notice that I/O lines connect to the display and also activate or deactivate the analog channels. When one analog-input channel activates through one I/O line with the output in the low state, the other lines are high-impedance inputs, which deactivate all other channels. Meanwhile, the display is off.

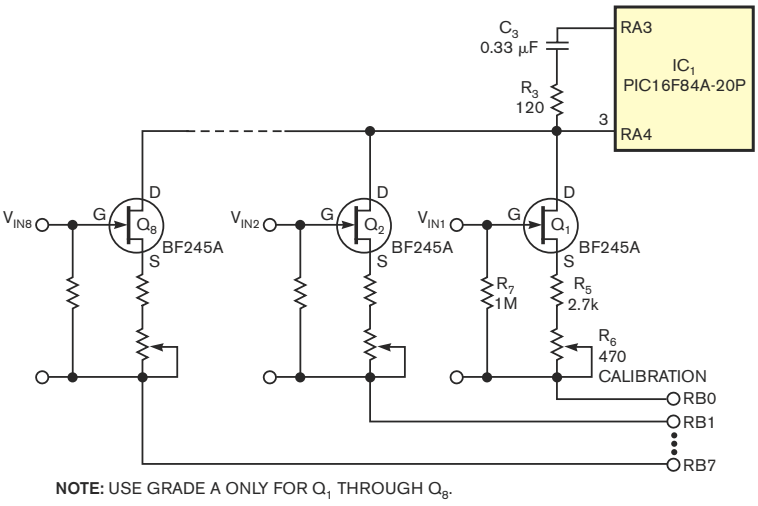

Figure 2 You can expand the number of voltages measured in Figure 1 by multiplexing additional transistor circuits.

The circuit in **Figure 1** also adds a simple serial link with no added components. If you connect two I/O lines, RA1 and RA2, configured as outputs, to RXD (Pin 2) and GND (Pin 5) of an RS-232 connector, you can reproduce, by software, positive and negative voltages with respect to ground of the PC's RS-232 port. When RA1 is high and RA2 is low, then RXD has a positive voltage of 5V with respect to ground of the PC's RS-232 port. When RA1 is low and RA2 is high, then RXD has a negative voltage of −5V with respect to ground of the PC's RS-232 port. **Listing 1**, available at www.edn.com/070510di1, gives a practical example with a PIC16F84A-20P. It is not optimized but is fully commented to make it easy to translate to another Microchip (www.microchip.com) midrange device, such as a PIC16F628A, that supports a frequency of 20 MHz with more I/O lines. EDN

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1 Benabadji, Noureddine, "Microcontroller, JFET form low-cost, two-digit millivoltmeter," *EDN*, June 22, 2006, pg 71, www.edn.com/article/CA6343251.
2 Benabadji, Noureddine, "Ultralow-cost, two-digit counter features few components," *EDN*, Aug 17, 2006, pg 69, www.edn.com/article/CA6360316.

Simple test setup performs functional testing of linear, single-cell lithium chargers

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Most currently available battery chargers are switched-mode types. Yet, a niche application exists for modern lithium-ion, single-cell linear-IC chargers, which have per-cell voltage of 4.2V. Further, the 5V-dc supplies, which are convenient for supplying single lithium-cell chargers, are ubiquitous. A linear charger charges the lithium cell from the 5V supply voltage at an efficiency, η, of approximately 4.2V/5V, or 84%. Although this value is ideal, the practical value is somewhat lower because of the power consumption of the charger's control circuitry. However, its efficiency is comparable with that of the switched-mode chargers. Linear chargers also provide some additional

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LT1494	LT1495	LT1496	1.5	2.7	375	1.2	2.1 to 36
LT1672	LT1673	LT1674	2	12	375	1.2	2.1 to 36
LT6000	LT6001	LT6002	16	50	750	5	1.8 to 16

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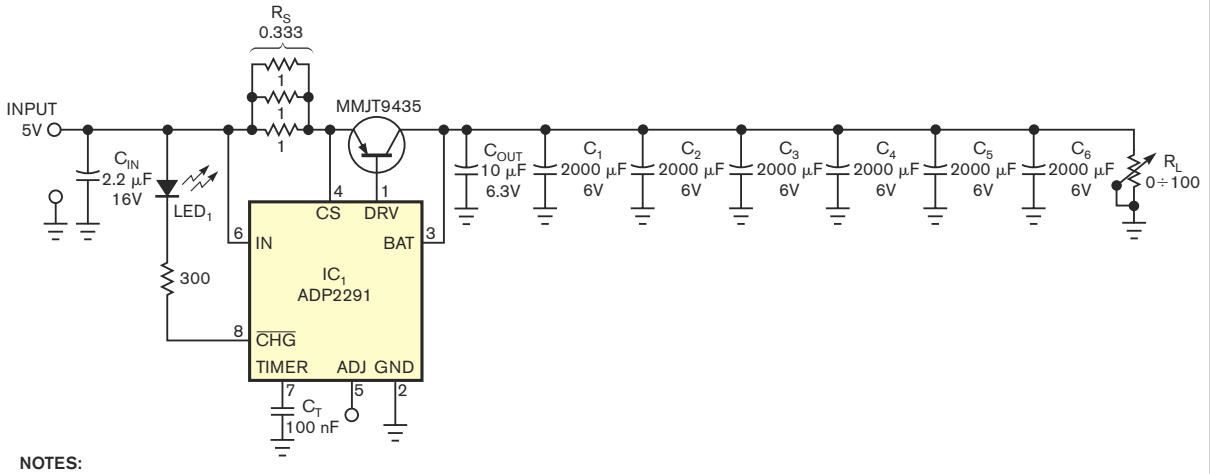

NOTES:
C_{IN} AND C_{OUT} ARE TANTALUM-CHIP CAPACITORS.
C_1 THROUGH C_6 ARE ALUMINUM-FOIL CAPACITORS.
C_T IS A CERAMIC-CHIP CAPACITOR.
LED_1 IS A 0805-SIZE, RED-CHIP LED.

Figure 1 A handful of off-the-shelf components allows you to qualitatively and quantitatively check the operation of a linear lithium single-cell charger.

benefits. They produce almost no EMI (electromagnetic interference), they require no inductors, and they require fewer capacitors than do switched-mode chargers.

The test setup in **Figure 1** employs IC_1, an Analog Devices (www.analog.com) ADP2291 for a lithium-cell linear charger. The device comes in 3×3-mm LFCSPs and QFN packages. The otherwise-welcome small dimensions of this IC pose an inspection problem. After soldering in the IC, you must perform a functional test of the charging circuit. You cannot rely on a visual inspection of solder joints, which are 0.5 mm apart.

In the charger circuit in **Figure 1**, for testing purposes, a bank of electrolytic capacitors substitutes for the lithium cell, dramatically reducing the charging interval and cutting the test time to seconds. Additionally, charging a capacitor has a well-defined course, and you can easily delete all previous charging and discharging by metallically short-circuiting the capacitor.

Also, a linear charger allows you to discharge the capacitor to 0V, which a lithium cell does not. After powering-on the circuit, you should momentarily light and then dim the LED annunciator to ensure that the charger is properly functioning. You estimate the time that the LED is on using the following **equation**:

$$t_{LEDON} \approx C\left(\frac{V_T}{I_{PR}} + \frac{V_{OUT}-V_T}{10I_{PR}}\right) = \frac{C}{I_{PR}}(9V_T + 1V_{OUT}),$$

where V_T is 2.8V, the threshold value of output voltage at which the charger enters its fast-charging mode; C is the total capacitance of the bank of capacitors that connect to output; I_{PR} is the precharge current; and V_{OUT} is 4.2V, the nominal output voltage at the end of the charging. The charge-current level is about 10 times that of the precharge mode. This condition occurs when you leave the ADJ (adjust) pin of the IC open. The first term in the parentheses of the **equation** corresponds to the precharge interval, and the second one expresses the charge interval. For a total capacitance of 0.012F, the precharge current is 46.5 mA, and the on-time of the LED is approximately 0.76 sec.

You can determine the value of the output threshold voltage by slowly turning the rotor of the variable-load resistor, R_L, from the minimum value of resistance until the LED dims. At that instant, you stop the rotor movement by disconnecting one end of the load resistor and measuring its value with an ohmmeter. The value of precharge current is then the output voltage divided by the measured value of the load resistor and the output voltage, or 4.2V. For the values of components in the **figure**, the experimentally determined value of a 44.4-mA precharge current is consistent with the typical value of 45 mA when the value of the current-sensing resistor is 0.33Ω (**Reference 1**).

You can measure the value of the threshold output voltage, V_T, as follows: Turn the rotor of the load resistor from minimum value of resistance while measuring the output voltage of the charger with a voltmeter. When the output voltage increases to about 2.6V, slowly proceed until the output abruptly changes to 4.2V. Using this method, you can determine the threshold voltage to be 2.75V. EDN

REFERENCE

1 "Compact, 1.5 A Linear Charger for Single-Cell Li+ Battery," ADP2291, Analog Devices, 2005, www.analog.com/en/prod/0%2C2877%2CADP2291%2C00.html.

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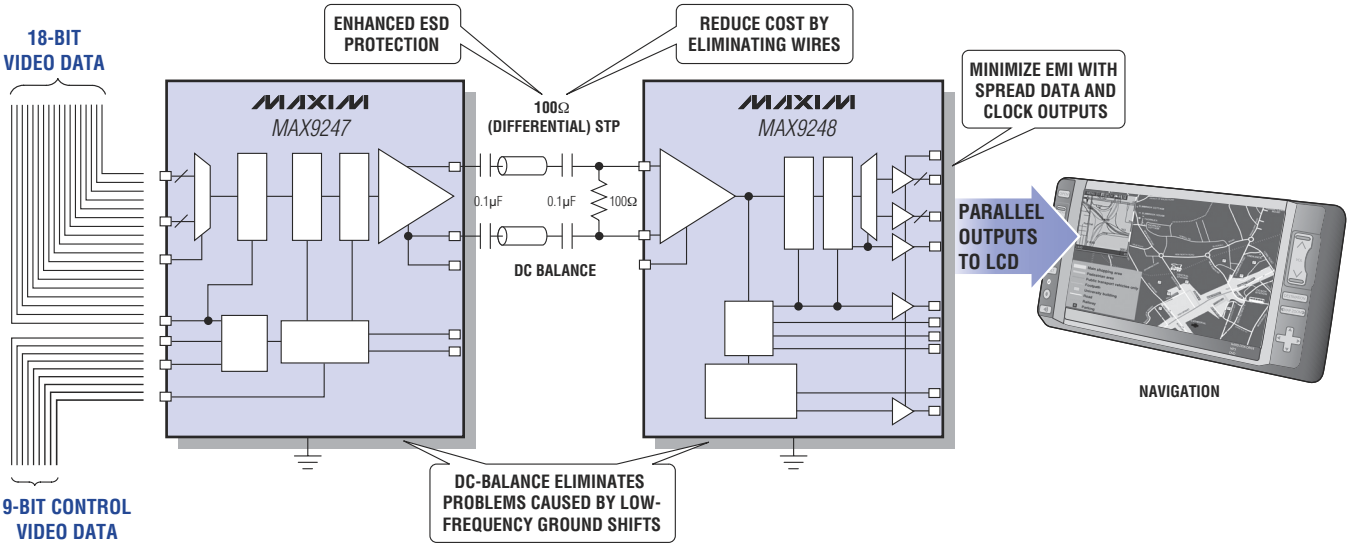

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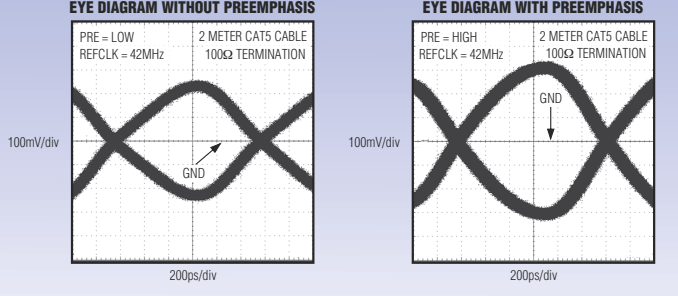

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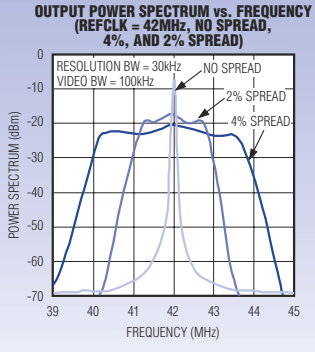

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Microcontroller provides low-cost analog-to-digital conversion, drives seven-segment displays

Name withheld by author's request

A previous Design Idea demonstrated how to use shift registers to increase a microcontroller's output capabilities (**Reference 1**). This expanded Design Idea provides low-cost analog-to-digital conversion and

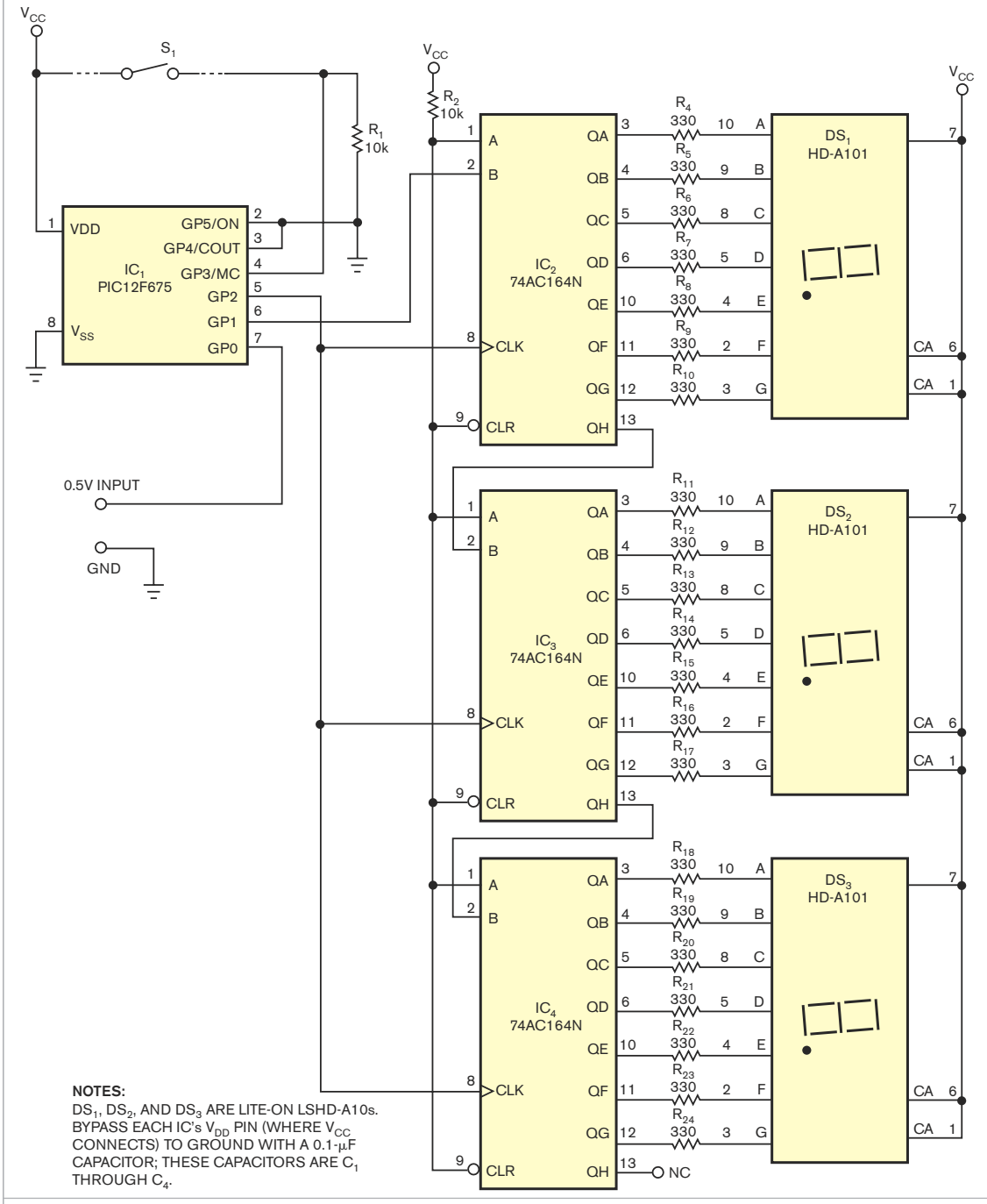

Figure 1 A low-cost microcontroller captures an analog voltage, converts it to a peak reading, and displays the results in decimal format on LED displays.

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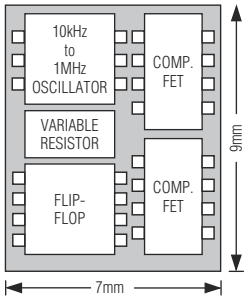

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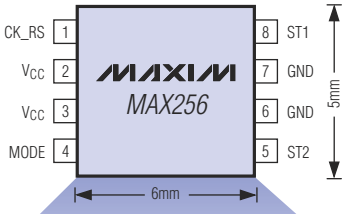

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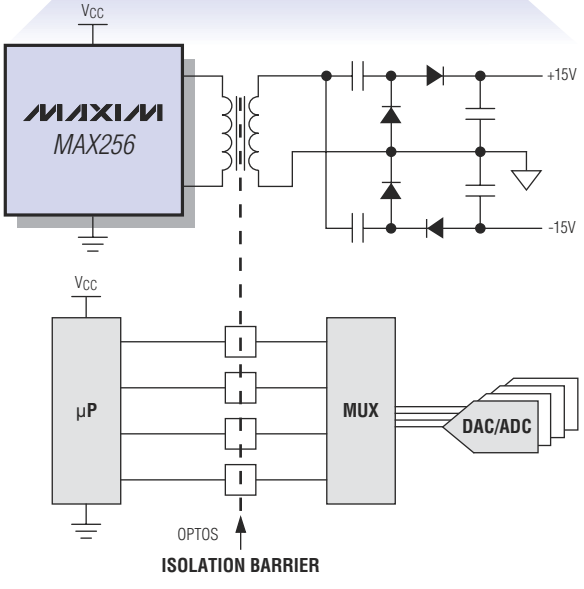

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a three-digit, seven-segment display. Although applicable to other microcontrollers, the circuit in **Figure 1** uses a Microchip (www.microchip.com) PIC12F675 controller and three multiply sourced 74AC164 serial-input/parallel-output shift registers.

The circuit accepts incoming signals of 0 to 5V. The microcontroller, IC_1, performs the analog-to-digital conversion and subsequently converts the binary-voltage value to BCD (binary-coded-decimal) format. Next, the microcontroller converts the BCD values to hardware-specific seven-segment-display masks and shifts the masks to the 74AC164 registers, IC_2 through IC_4, which in turn drive the seven-segment displays.

Available for downloading from the online version of this Design Idea at www.edn.com/070510di2, **Listing 1** implements an additional function. Instead of displaying each input value as it's converted, the microcontroller operates as a peak detector. When the maximum value changes, the microcontroller updates the three-digit display. A pushbutton switch, S_1, resets the maximum value. You can modify the code to apply other functions to the input data and calculate and display the data in other formats. In addition, you can modify the interrupt-driven conversion process to accommodate different sampling rates. When you modify the sampling rate or the ISR (interrupt-service routine), ensure that the ISR completes execution within a single sample period. EDN

INSTEAD OF DISPLAYING EACH INPUT VALUE AS IT'S CONVERTED, THE MICROCONTROLLER OPERATES AS A PEAK DETECTOR.

REFERENCE

1 Raynus, Abel, "Squeeze extra outputs from a pin-limited microcontroller," *EDN*, Aug 4, 2005, pg 96, www.edn.com/article/CA629311.

Amplifier cancels common-mode voltage

W Stephen Woodward, Chapel Hill, NC

Since the dawn of time—or at least since the dawn of precision electronics—a major headache for analog designers has been CMV (common-mode-voltage)-induced errors, also known as the dreaded ground loop. Although almost mystical is the fear it strikes in the hearts of engineers, there's nothing particularly mysterious about CMV. CMV errors occur for a simple reason: The common voltage references—that is, ground—of circuitry in different places, such as sensors in one chassis and an ADC in another, are apt to differ. Therefore, when you

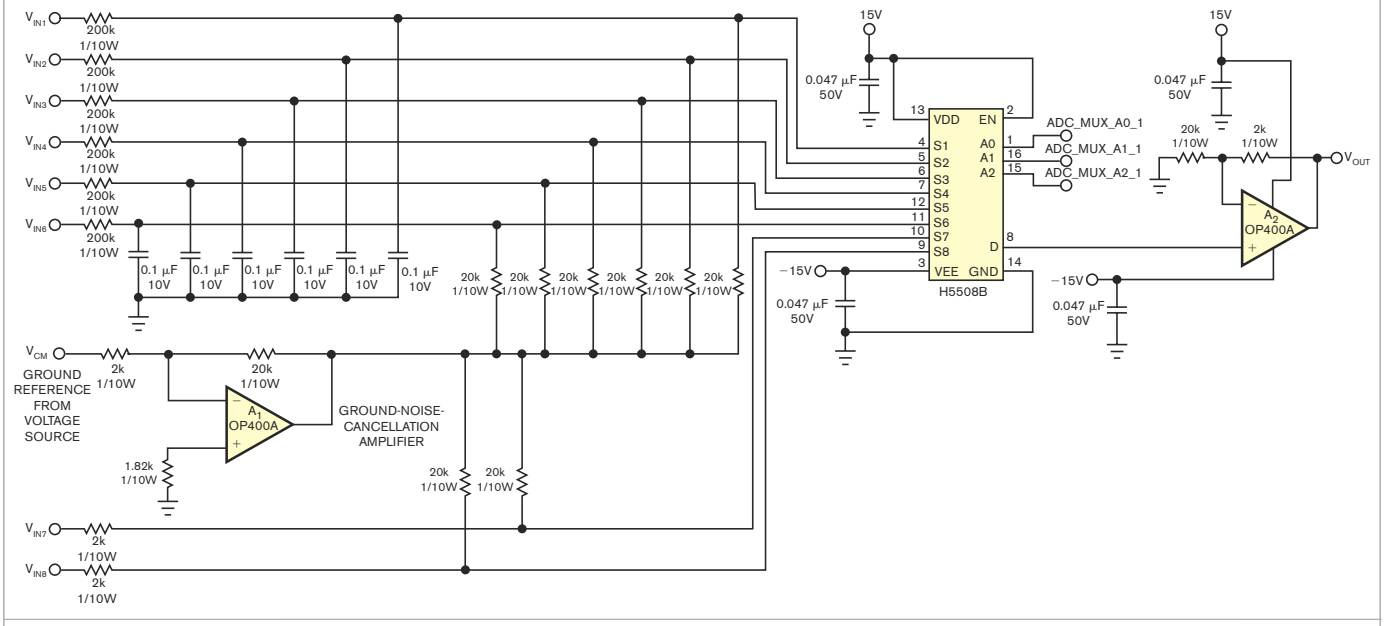

Figure 1 Amplifier A_1 amplifies and inverts the common-mode voltage by a factor of −10. Then, the circuit applies this signal to an array of passive summation networks. An analog multiplexer selects the desired input signal, and op amp A_2 supplies a compensating gain.

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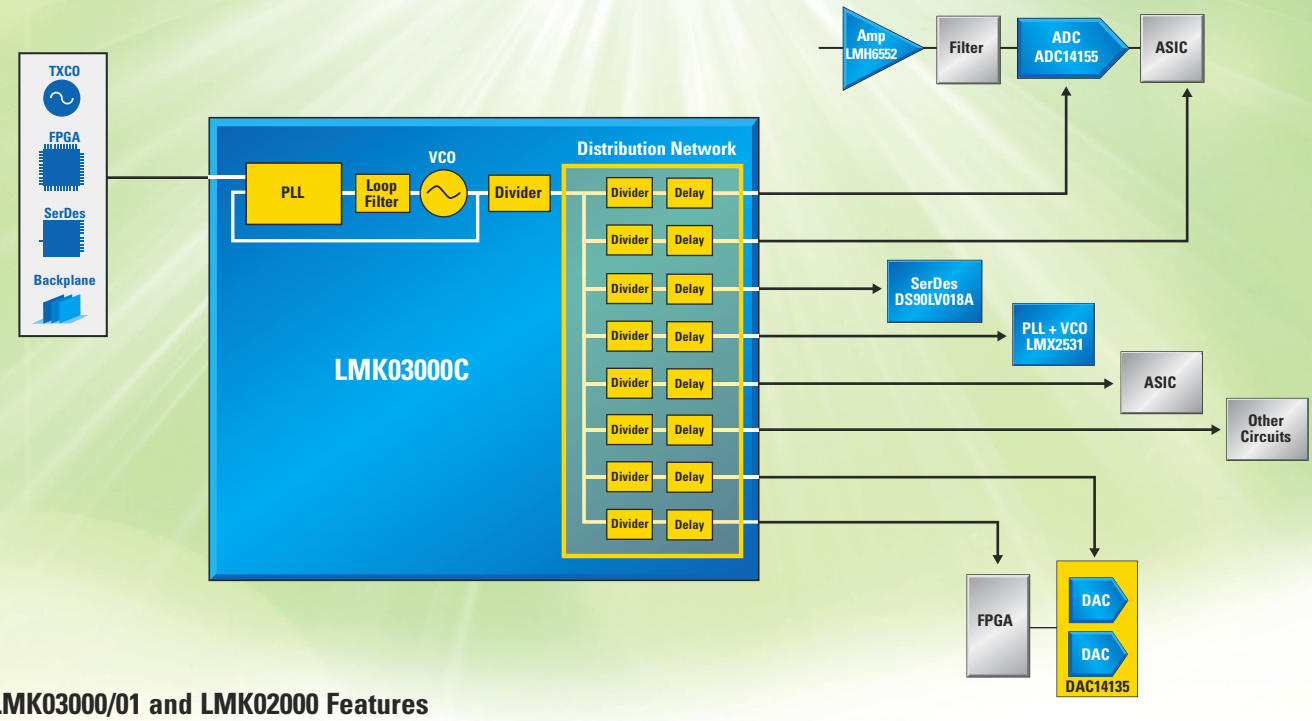

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route signals between remotely located circuits, the CMV differential appears as additive noise and offset, corrupting the desired signals.

Many approaches exist for eliminating CMV errors. These methods include the brute-force approach of using massive amounts of copper in ground interconnections, fully differential instrumentation-amplifier signal conditioners, and galvanic isolators. Each has its place, depending on such factors as the severity of the CMV problem and the number of signal channels needing CMV remediation. One of the most popular and effective CMV remedies is differential amplification, in which you perform an analog subtraction to remove the CMV component from the signal. The downside of this method is that it requires a dedicated amplifier for every signal channel. The circuit in **Figure 1** is a variation on that same differential-amplifier idea, but it combines two shared CMV amplifiers with simple passive-resistor

ONE OF THE MOST POPULAR AND EFFECTIVE CMV REMEDIES IS DIFFERENTIAL AMPLIFICATION, IN WHICH YOU PERFORM AN ANALOG SUBTRACTION TO REMOVE THE CMV COMPONENT FROM THE SIGNAL.

pairs among eight multiplexed channels to provide CMV cancellation for a large number of analog channels at minimum component count.

Here's how it works. Amplifier A_1 amplifies and inverts the CMV by a factor of −10. You then apply this CMV to an array of passive-summation networks—one for each input signal. The 10-to-1 ratio of the two legs of each network combines the incoming input-voltage and CMV signals with the –10V CMV ground-noise reference: $V=10/11\times(V_I+V_{CM})+1/11\times(10\times V_{CM})=10/11\times V_I+10/11\times(V_{CM}-V_{CM})=10/11\times V_I$. V_{CM} is attenuated by a factor depending mainly on the accuracy of 20- versus 2-kΩ resistor-ratio matching. For 1% matching, the CMRR (common-mode-rejection ratio) is approximately 100-to-1, or 40 dB; for 0.1% matching, CMRR is 1000-to-1, or 60 dB.

The analog multiplexer then selects the desired input voltage for input to the 11/10 scale-factor-correction amplifier, A_2. The optional 0.1-µF filter capacitors provide a modicum of low-pass noise filtering, and you should tailor them for the bandpass requirements of your application. The approximately 180 µsec, or approximately 88 Hz, is too slow for many applications and too fast for others. EDN

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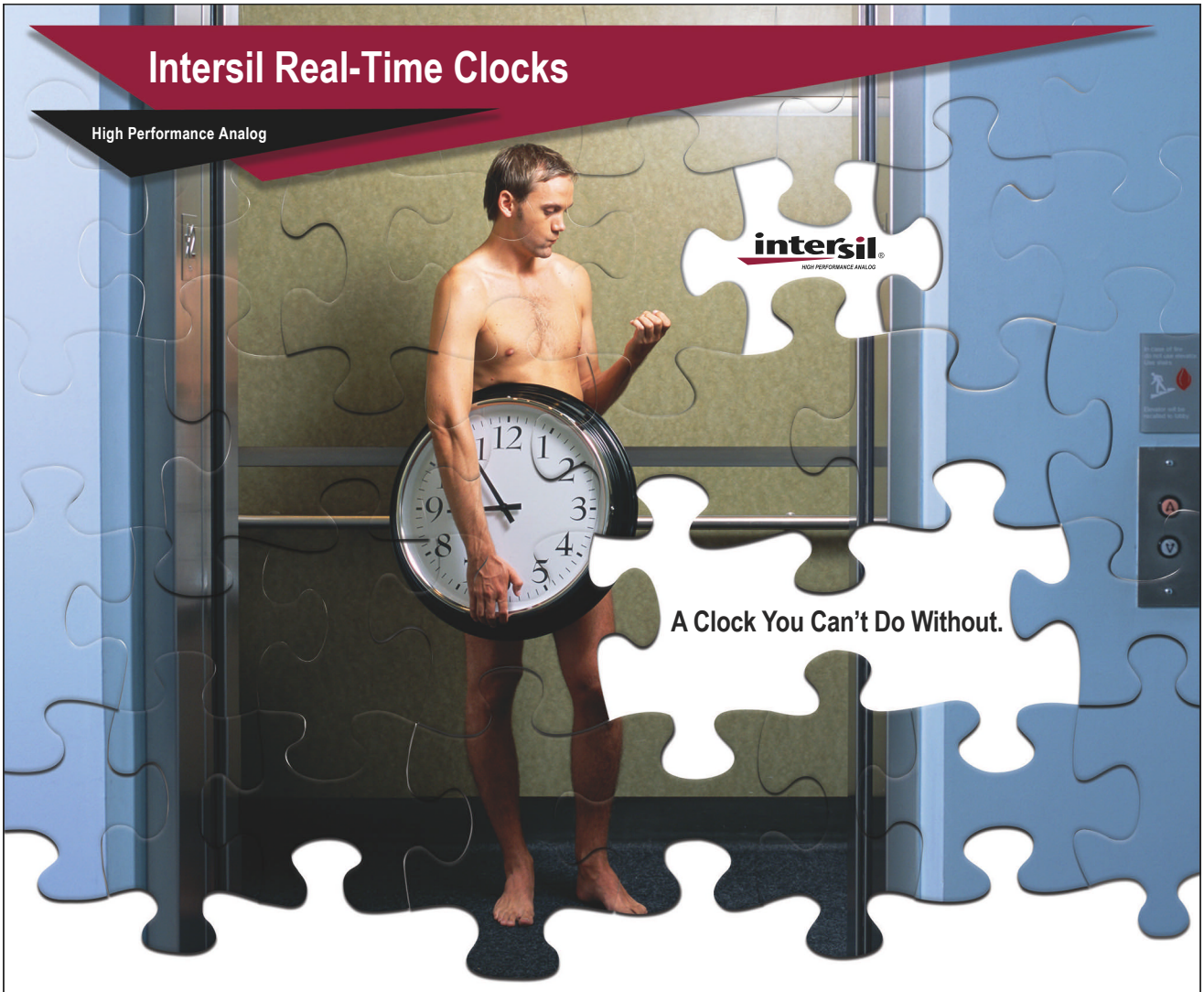

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BRIEF

Selecting the Correct IC for Power-Supply Applications

By William Hadden

Applications Engineer, High Performance Analog, Low Power DC/DC

Introduction

To select the correct IC(s) for the job, many factors such as cost, solution size, power source, duty cycle, and required output power must be weighed and ranked by importance. This article covers the rationale for the application solution shown in Figure 1.

This example application is portable, requires the lowest possible battery consumption and a small form factor, and operates from a single-cell Li-ion battery that is charged whenever the 12-V supply is available. While it is desirable to minimize cost, small size and high efficiency for extended battery life are often more important.

Choosing the Topology

Due to the space constraints of this application, using LDOs would be considered first but may not always be possible due to power dissipation and efficiency constraints. Beginning with the 5-V, 2-A rail, it is clear that a switching converter should be used because the power dissipated by an LDO, in this case 14 W, is excessive. For this rail, an inductive step-down converter is the best choice.

Now consider the battery charger. This battery is charged from the 5-V rail. The application has a single-cell Li-ion battery that has a charging voltage of 4.2 V. With the space constraints of the application, a linear charger is a good choice. The charging efficiency is not as much of a concern because the only time this device will operate is when the 12-V power adapter is available. However, when selecting the peak charge current of a battery deeply discharged to 3 V, take care to limit the thermal dissipation of the device.

- For the 3.3-V rail, a switching converter is the best choice due to the large output current required.
- For the 1.50-V rail, either a switching step-down converter or an LDO would be acceptable. With the latter, efficiency would be in the 25% range and would require an input current of 100 mA. Substituting a switching step-down converter can provide efficiencies higher than 90%, which require an input current of 30 mA. There are many very small switching-converter solutions that can supply the required output power, so the size increase over an LDO circuit is not appreciable. To maximize battery life, the step-down converter is a better choice.
- For the 2.5-V rail, again, either topology is acceptable. Due to the low current requirements and lower input/output differential, an LDO is the best choice for the smallest size.

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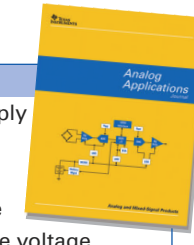

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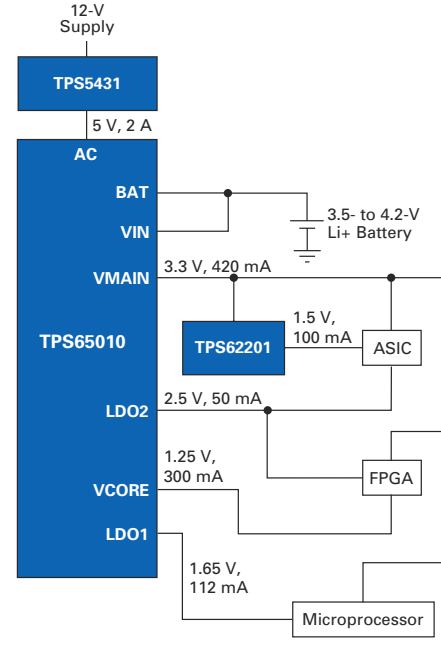

Figure 1: Power-Supply Solution

- For the 1.25-V rail, a switching converter is the best choice. With the high (300-mA) load requirement and the large input/output differential, an LDO would dissipate too much power and is too inefficient.
- For the 1.65-V rail, again, either topology is acceptable. The same logic as for the 1.50-V case makes a switching converter a possibility, but other factors discussed later require that this be an LDO.

Selecting the Best IC(s) for the Job

Taking size and cost constraints into consideration, the chosen ICs should be as highly integrated as possible and should contain internal MOSFETs. This saves on solution size as well as on production costs. There are also multi-output ICs available that decrease the solution size even further.

The best solution for the 5-V rail is the TPS5431, shown in Figure 1. Its wide input range (5.5 to 23 V) will accept the 12-V, ±10% input. The TPS5431 also provides up to 3 A with an adjustable output voltage down to 1.2 V. The switching MOSFET and the compensation components are integrated, and the 95% efficiency meets the battery-power demands. The device comes in the SO-8 package for a very small solution size.

There are several choices for the battery charger. The bq24010, a small battery charger IC in the 3 x 3-mm QFN package, is a good choice. Its solution size is very small and requires only three external components, but there is a better solution. The TPS65010 is a power- and battery-management IC for Li-ion-powered systems. This IC integrates two switching converters (VMAIN and VCORE), two LDOs (LDO1 and LDO2), and a single-cell Li-ion battery charger. In addition to these rails, the IC also eliminates the need for a switchover circuit when the 12-V power adapter is connected. In this application, VMAIN powers the 3.3-V rail, VCORE powers the 1.25-V rail, LDO1 powers the 1.65-V rail, and LDO2 powers the 2.5-V rail. Using the TPS65010 drastically reduces the solution size as well as the external component count.

The remaining 1.50-V rail can be powered from a step-down switcher such as the TPS62201. This device comes in a five-lead SOT-23 package and requires only three external components (input/output capacitors, inductor, and two feedback resistors). This translates to a very small solution size. To increase efficiency, the input of this device should be connected to the 3.3-V MAIN output of the TPS65010.

Calculating the System Efficiency

For this discussion, it has been assumed that all of the voltage rails are on 100% of the time, which is rarely the case. Sometimes, where an inductive switcher would typically be used, an LDO may be an acceptable choice to minimize solution size. Calculating the efficiency difference between each topology determines which to use.

The percentage of time that an output is enabled (the duty cycle) can be used to determine the effect of each rail on the total solution efficiency. First, the effective total output power is calculated by summing up the effective power for each rail:

$$P_{OUTEFFTOT} = \sum_{i=1}^{n} D_i \times P_i,$$

where P_i is the output power from one output rail and D_i is the duty cycle for the same rail. Next, the power lost by each rail is calculated:

$$P_{LOSS} = D \times P_{RAIL}\left(\frac{1}{\eta_{RAIL}} - 1\right)$$

Summing up the power loss for all of the rails provides the total power loss:

$$P_{LOSSTOTAL} = \sum_{i=1}^{n} D_i \times P_i\left(\frac{1}{\eta_i} - 1\right),$$

where η_i is the efficiency of the individual output rail. The effect of each rail on the overall system efficiency can then be calculated:

$$\eta_{SYSRAIL} = \frac{D \times P_{RAIL}}{P_{LOSSTOTAL} + P_{OUTEFFTOT}}$$

The total system efficiency can be determined by summing all of the rail system efficiencies or by using the following equation:

$$\eta_{SYS} = \frac{P_{OUTEFFTOT}}{\sum_{i=1}^{n} \frac{D_i \times P_i}{\eta_i}}$$

As the duty cycle for an output increases, the calculation of solution size versus efficiency must be examined to determine the optimal solution. For example, with the 3.3-V, 420-mA output on all the time, using an LDO instead of an inductive switcher would reduce the overall efficiency by nearly 4%. If the 3.3-V output was enabled for only 10% of the operation time, then using an LDO instead of a switcher would result in a drop of less than 0.75% in overall efficiency. These two cases are clearly extremes but illustrate how the duty cycle affects the overall efficiency.

Conclusion

Requirements such as available space, available input power, output power, duty cycle, and cost all must be examined to choose the best solution. Start by ranking the requirements by importance, then select the topology for each output based on the requirements. Finally, choose the most cost-effective solution for each output. Following these simple steps should take the difficulty out of power-supply design.

References:

1. TPS5431 Datasheet (SLVS632C)
2. TPS65010 Datasheet (SLVS149B)
3. TPS62201 Datasheet (SLVS417E)

productroundup

SENSORS AND TRANSDUCERS

Magnetic encoders aim at angular detection

Available in 10- or 12-bit resolutions, the AEAT-60xx magnetic-encoder series suits angular detection within 360°. The encoders feature absolute-angle detection upon power-up with a 0.35° resolution for the 10-bit version and a 0.0879° resolution for the 12-bit version, equivalent to 4096 and 1024 positions per revolution, respectively. Additional features include an SSI (synchronous-serial-interface) output for absolute-position data in binary format, a 3.3 to 5V power supply, a −40 to +125°C temperature range, and a ±1-LSB code-monotony error. The series comes in 23-mm-tall cylinders with 23-mm diameters, and prices range from $18 to $20 (1000).

Avago Technologies, www.avagotech.com

Flow sensors measure airflow and gas-flow speeds using a thermopile

The D6F MEMS (microelectromechanical-system) flow sensors use thermopiles to convert thermal energy into electrical energy. The use of a thermopile allows them to measure airflow and gas-flow speed from 1 mm/sec to 40m/sec. Typical flow sensors use a resistance-measurement method by tracking the electrical-resistance change of a material according to its change in temperature, requiring adjustment of the resistance balance. The sensors operate from −10 to +60°C, have a 12 to 24V-dc supply voltage, and consume 15 mA. Measuring 15×20×60 mm, the devices also feature an integral orifice with a 1 to 5V-dc analog output. The D6F-01A1-110 has an airflow range from 0 to 1L/minute and costs $72.41 (100); the D6F-20A5-00 has an airflow range from 0 to 20L/minute and costs $125.40 (100).

Omron Electronic Components, www.components.omron.com

Ultrasonic-sensor family has programmable start and stop voltages

The M-300 ultrasonic-sensor family provides precision noncontact distance measurement for factory-automation or industrial-process control. Operating from 12 to 24V dc, the family includes varying ultrasonic frequencies producing detection ranges of 100 mm to 4.5m. The 0 to 10V-dc linear output is proportional to the measured distance to the target from the minimum-detection distance to the nominal-maximum-target distance. The device features a reprogrammable start and finish output-voltage range of 0 to 10V dc, a corresponding target-distance span that is programmable to start and stop at two target ranges, and a programmable output voltage operating as a digital switch at a specified setpoint distance. Prices for the MassaSonic M-300 series range from $200 to $400, depending on model.

Massa Corp, www.massa.com

MEMS-sensor family has three axes of sensitivity

Providing three axes of sensitivity, the MMA73x0L XYZ-axis accelerometers have a 3-µA sleep mode. Features include 400-µA power consumption, a 2.2 to 3.6V operating voltage, a 1-msec power-up response time, a 0.5-msec response time, and a self-test function. The MEMS (microelectromechanical-system)-sensor devices include the MMA-7360L, the MMA7340L, and the MMA-7330L with selectable 1.5 to 6, 3 to 12, and 4 to 16g sensitivity ranges, respectively. Available in 3×5×1-mm LGA

SENSORS AND TRANSDUCERS

packages, the sensors cost $3.66, $3.59, and $3.53, respectively.
Freescale Semiconductor, www.freescale.com

Accelerometer gauges values on three axes

Joining the vendor's family of ultracompact low-g linear accelerometers, the LIS302ALK axis accelerometer measures acceleration values for the x, y, and z axes. The low-power MEMS (microelectromechanical-system) device provides an analog output, with a ±2g output range, suiting low-frequency vibration monitoring at low power consumption. Features include a power-down mode reaching 1-µA supply current and built-in self-test, allowing customers to verify the functioning of the sensor after assembly on the board. The motion sensors also suit devices that need to power on or off by activating a remote control during or after a user touches or moves them, controlling the overall power consumption of the circuitry. The family also aims at medical applications, monitoring motion or detecting the position or activity level of patients. Available in a 5×3×0.9-mm plastic package, the ultracompact design provides shock survivability as high as 10,000g in 0.1 msec. The LIS302ALK costs $2.95 (30,000).
STMicroelectronics, www.st.com

TEST AND MEASUREMENT

Trace module provides fine-tune code performance

The nonintrusive, hardware-based XDS560 trace module features advanced visibility and capabilities for debugging specialized problems in high-performance, real-time embedded-system applications. The trace tool provides fine-tuning code performance and cache optimization of complex multichannel applications. The device comprises Blackhawk's XDS560 high-speed USB emulator and the vendor's trace module with a high-density, 60-pin header connector. Compatible with the TMS320C6455 SRIO EVM (evaluation module), the TMS320DM642 EVM, and the TMS320C6416T DSK (design starter kit), the development tool costs $9995.
Texas Instruments, www.ti.com

Embedded-system monitoring tool displays data numerically or graphically

The uC/Probe-STD universal tool enables developers to monitor embedded systems in a live environment. Aiming at 8-, 16-, 32-, and 64-bit processors, DSPs, and compilers, the tool suits use with any tool chain generating an .ELF file, eliminating the need for custom programming or scripting. The tool graphically displays data on a computer running Microsoft Windows, and users can display values numerically or as gauges, bar graphs, plots, graphs, LEDs, counters, or pie charts. The visuals are high-quality enough for use in system diagnostics or as a final-product user interface, allowing users to monitor the status of a device remotely. The uC/Probe-STD embedded-system monitoring tool costs $495 per seat.
Micrium, www.micrium.com

Payload card combines waveform generation with FPGA-based DSP

Combining FPGA-based DSP technology with seven channels of high-resolution-waveform generators, the Janus XVS features digital-to-analog conversion at 16-bit resolutions and 500M-sample/sec clock rates per channel in a VXS payload-card form factor. The converters link into a Xilinx FPGA with an advanced 5-Gbyte DDR-SDRAM architecture. This architecture supports storage of digitized or generated high-resolution waveforms for replay through the DAC channels. The programmable FPGA supports advanced real-time digital-signal processing and triggering, implementing immediately before the DAC outputs. The Janus VXS payload card costs $19,900.
Tek Microsystems, www.tekmicro.com

Recording-and-development software supports RAID and JBOD arrays

Targeting the vendor's family of RTS systems, the Model 4990 SystemFlow real-time recording-and-development software provides features for controlling data-acquisition and recording functions. Joining the vendor's software suite, File Manager and Signal Viewer have enhanced display and analysis functions. Additional support includes RAID (redundant-array-of-inexpensive-disks) and JBOD (just-a-bunch-of-disks) Fibre Channel arrays, providing a 6-Tbyte or greater real-time-recording capacity. The RTS system costs $26,995, and the Model 4990 SystemFlow software costs $8500.
Pentek, www.pentek.com

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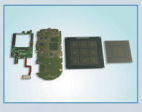

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EDA TOOLS

Hierarchical-design tool features PinAhead technology

Version 9.1 of the PlanAhead hierarchical-design and -analysis software supports Virtex-5 LXT and SXR families of 65-nm FPGAs, as well as Spartan-3 and nonvolatile Spartan-3AM platforms. The vendor's PinAhead technology allows users to automatically or semiautomatically assign I/O ports to physical package pins. Designers can assign interface-I/O groups to I/O pins by dragging them into graphical representations of FPGAs. Thus, designers can begin pin assignment before completing a PCB (printed-circuit board) or an FPGA netlist. Engineers can also create their own port lists with a GUI, or they can import a CSV (comma-separated-values) spreadsheet. Improved dynamic-placement constraints allow users to assign the constraints or import them from a netlist that the company's ISE design tools generate. Designers can also clear placement constraints without affecting remaining user constraints; they can selectively mark a subset of the placement constraints that the ISE implementation tools assign. The tool then treats these placement constraints as user-defined constraints. A single-user license costs $2495.

Xilinx, www.xilinx.com

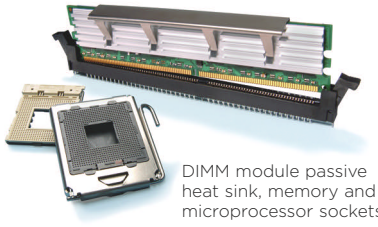
Advanced synthesis-tool suite supports Spartan-DSP series

The Precision Synthesis 2006a2 suite of advanced synthesis products supports Xilinx's Spartan-DSP series, and support for the vendor's LeonardoSpectrum tool suite will follow. The suite features support for ASIC prototyping, including DesignWare libraries, SDC (Synopsys Design Constraints), and gated-clock handling. The tool also provides implementation and optimization techniques, such as automatic mapping and inferencing of dedicated DSP and RAM blocks. The Precision Synthesis 2006a2 tool suite costs $17,600.

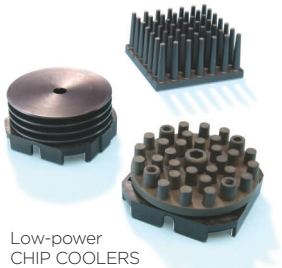
Mentor Graphics, www.mentor.com

RF- and microwave-design software automates documentation

The most recent version of Genesys RF- and microwave-design software features the LiveReport tool,



DIMM module passive heat sink, memory and microprocessor sockets



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Agilent Technologies, www.agilent.com

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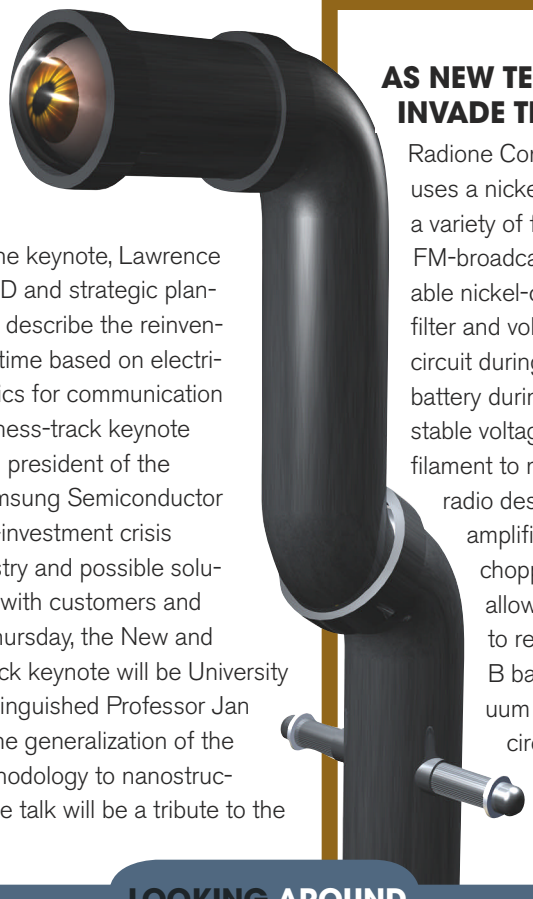
LOOKING AHEAD

TO DAC 2007

The 44th annual DAC (Design Automation Conference) begins on June 3 in San Diego. This year's special theme and Monday keynote concern automotive electronics. In the keynote, Lawrence Burns, vice president of R&D and strategic planning at General Motors, will describe the reinvention of the automobile, this time based on electrical propulsion and electronics for communication and control. Tuesday's business-track keynote will feature Oh-Hyun Kwon, president of the Systems LSI division of Samsung Semiconductor Business, on the return-on-investment crisis facing the electronics industry and possible solutions through collaboration with customers and technical breakthroughs. Thursday, the New and Emerging Technologies Track keynote will be University of California—Berkeley Distinguished Professor Jan Rabaey offering a talk on the generalization of the semiconductor-design methodology to nanostructures and bio structures. The talk will be a tribute to the late Richard Newton, PhD.



LOOKING BACK

AS NEW TECHNOLOGIES INVADE THE RADIO

Radione Company of Vienna, Austria, uses a nickel-cadmium storage cell for a variety of functions in a portable AM/FM-broadcast receiver. The rechargeable nickel-cadmium cell serves as a filter and voltage stabilizer in the filament circuit during ac operation, as a spare A battery during battery operation, and as a stable voltage source for the mixer tube filament to minimize frequency drift. The radio design uses transistors as audio amplifiers and B+ power-supply choppers to reduce current drain, allowing four conventional D cells to replace the customary dry-cell B battery. The set employs vacuum tubes in the high-frequency circuits and germanium diodes for AM and FM detectors.
—*Electrical Design News*, May 1957

LOOKING AROUND

AS THE US CONGRESS PONDERS PATENTS

On the principle that no one is safe while the Congress is in session, we look with concern as that august body takes up once again the question of the US patent system. The growing fury across the industry and the investment community over the impact of patent trolls triggers, one presumes, this new examination. Industry leaders—a notoriously reticent group when it comes to politics—are becoming increasingly vocal about the patent system's suppression of creativity and its toxic effect on new ventures. One remembers, however, that we gained the current system through what was at the time called patent reform.

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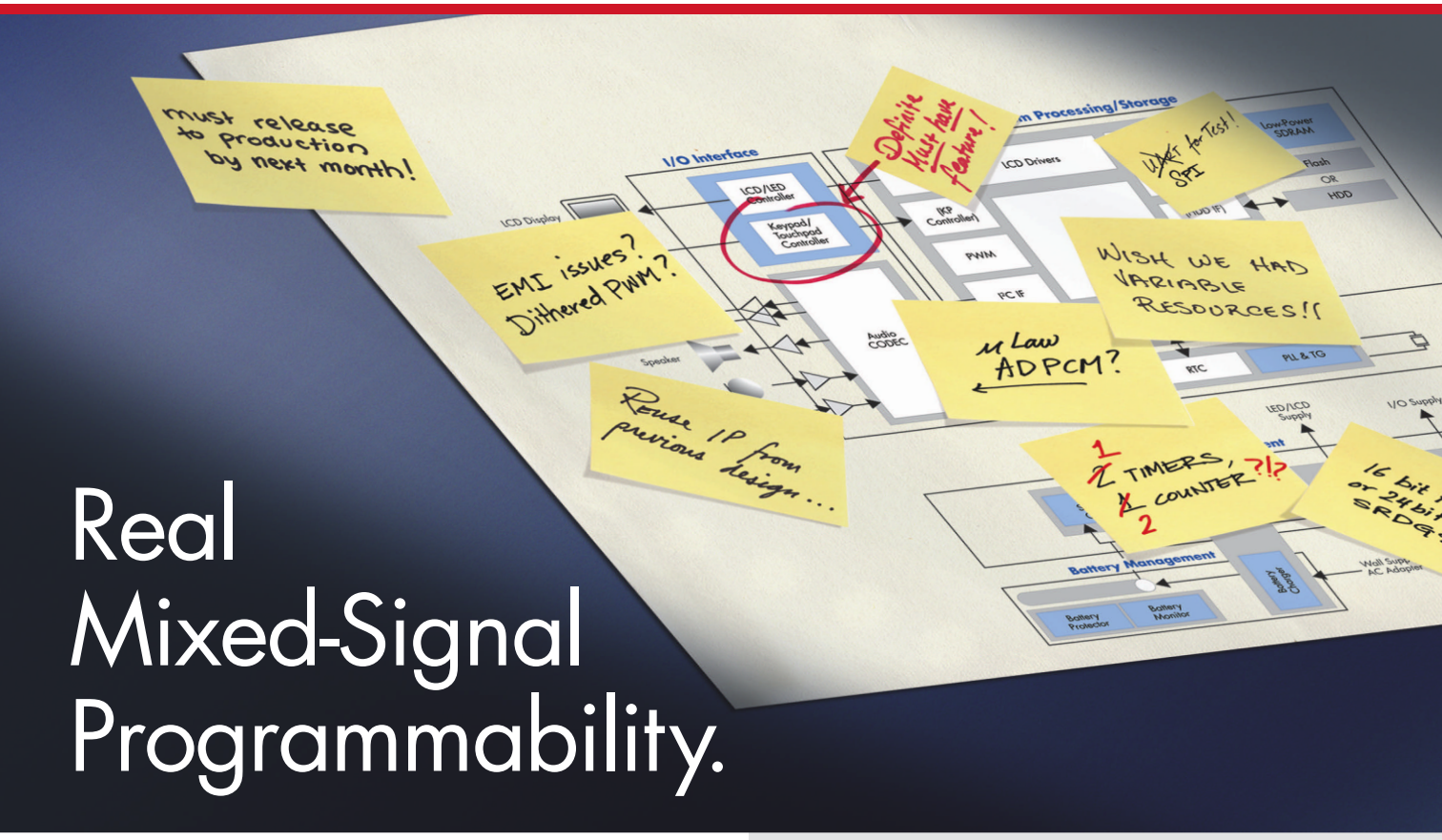

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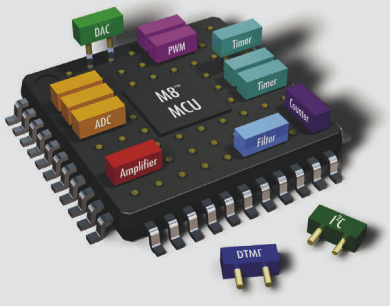

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